CH390 Datasheet

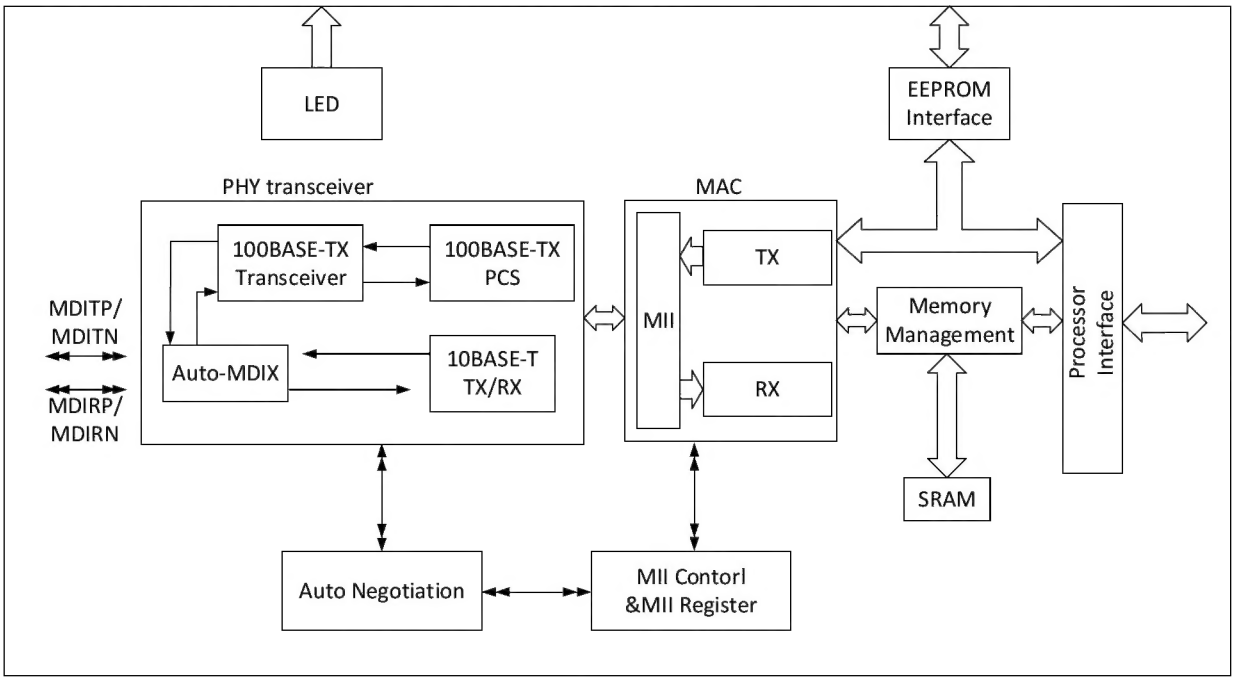
V1.7

https://wch-ic.com

1. Overview

CH390 is an industrial-grade Ethernet controller chip with its own 10/100M Ethernet Media Access Controller (MAC) and Physical Layer (PHY), supporting CAT3, 4, 5 for 10BASE-T and CAT5, 6 for 100BASE-TX connections, supporting HP Auto-MDIX, low-power consumption design, and complying with IEEE 802.3u specification. CH390 has built-in 16K bytes SRAM, supports parallel interface and SPI serial interface for compatibility with various MCUs, MPUs, DSPs and other controllers.

The following figure shows the block diagram of CH390.

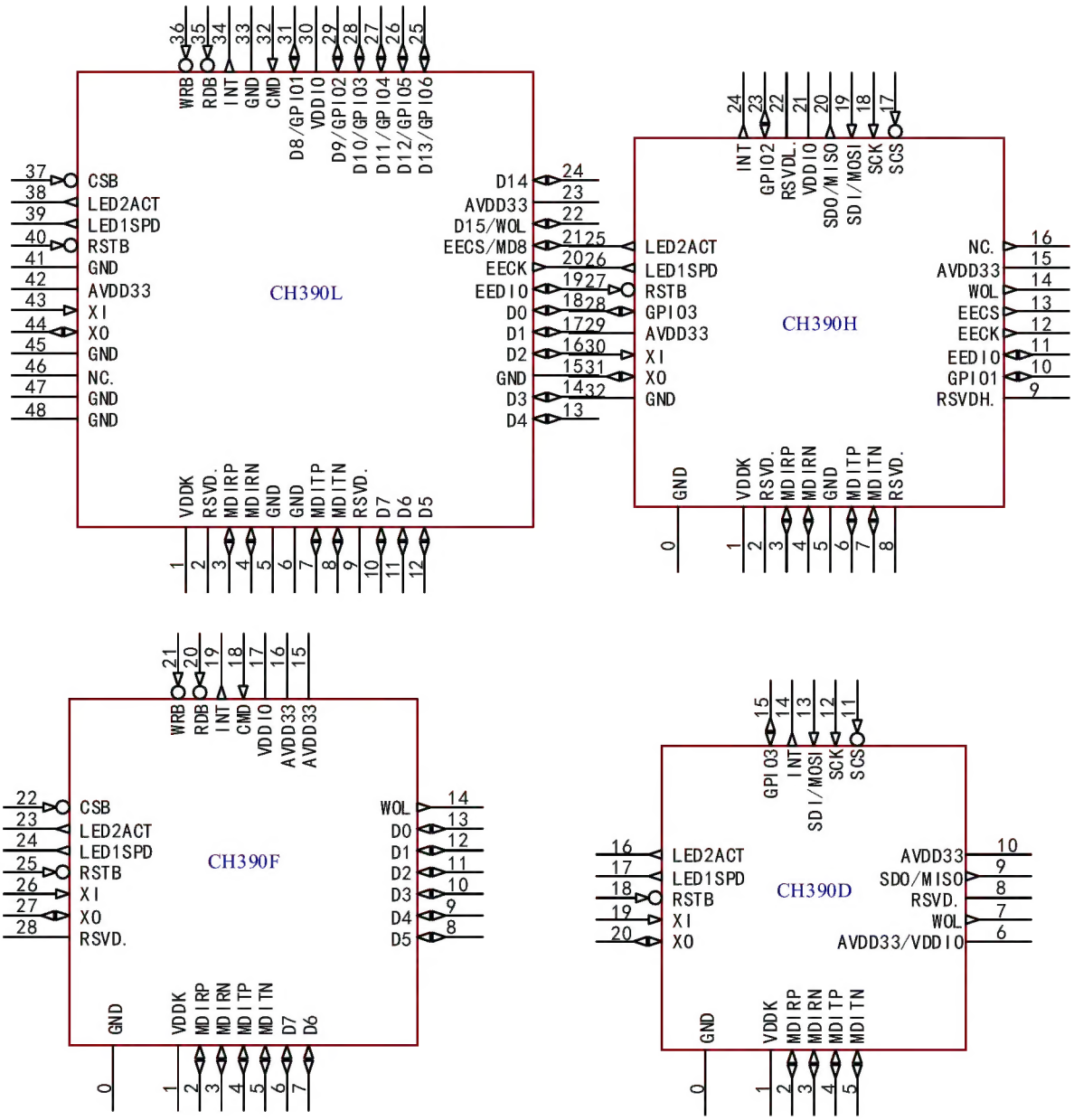


2. Features

- It comes with its own internal Ethernet Media Access Controller (MAC) and Physical Layer (PHY).
- CH390L supports 8-bit and 16-bit parallel interface, CH390F supports 8-bit parallel interface, CH390H and CH390D supports SPI serial interface.
- Built-in unique Ethernet MAC address, no additional purchase or distribution, no external EEPROM.
- CH390H/D provides SPI slave interface, supports SPI clock modes 0 and 3 with clock speeds up to 72MHz.
- Integrated low-power 10/100M transceiver based on DSP algorithm implementation transceiver.
- Support Auto-MDIX to exchange TX/RX and automatically identify positive and negative signal lines.
- Support 10BASE-T and 100BASE-TX and Auto-Negotiation.
- Support UTP CAT5, CAT6 twisted pair cable, support 120 meters transmission distance.
- Support wake-up frames, link state changes, and magic packet events for remote wake-up.
- Support IEEE 802.3x flow control.
- Support IPv4 TCP/UDP and IPv6 TCP/UDP checksum generation and checking.

- Built-in LDO, CH390F/H has independent I/O power supply pin VDDIO, supporting 1.2V to 3.3V interface voltage.
- Built-in 50Ω matching resistor, built-in crystal oscillator capacitor, with lower BOM cost.
- Support optional external EEPROM configuration chip.
- Small-size QFN20, QFN28, QFN32 and LQFP48 packages are available.

3. Pinouts



Package Form	Body Size	Pin Pitch		Package Description	Order Model
QFN20	3.0*3.0mm	0.40mm	15.7mil	Quad Flat No-Lead Package	CH390D
QFN28	4.0*4.0mm	0.40mm	15.7mil	Quad Flat No-Lead Package	CH390F
QFN32X5	5.0*5.0mm	0.50mm	19.7mil	Quad Flat No-Lead Package	CH390H
LQFP48	7.0*7.0mm	0.50mm	19.7mil	Low Profile Quad Flat Pack	CH390L

Note: 1. Pin 0# refers to the EPAD of the QFN package.

2. 2. It is recommended that CH390D and CH390F are preferred for their small size.

3.CH390 is divided into early VDDK discrete version and later VDDK merged version, the main difference is: merged version will be shorted to VDDK inside AVDDK when packaged, merged version is forward compatible with the discrete version, the CH390 with the batch number countdown 6 digit of 0 or lot number countdown 5 digit of 2 is the discrete version of VDDK, or else it is the merged version.

4. Pin Definitions

CH390D Pin No.	CH390F Pin No.	CH390H Pin No.	CH390L Pin No.	Pin Name	Type	Pin Description
2/3	2/3	3/4	3/4	MDIRP/ MDIRN	I/O	Differential input in 10BASE-T/100BASE-TX MDI mode. Differential output in 10BASE-T/100BASE-TX MDIX mode.
4/5	4/5	6/	7/8	MDITP/ MDITN	I/O	Differential output in 10BASE-T/100BASE-TX MDI mode. Differential input in 10BASE-T/100BASE-TX MDIX mode.
1	1	1	1	VDDK	P	The external 1uF capacitor to ground is placed close to the chip.
-	-	2	2	RSVD.	P	Reserved, and it is suggested to short to VDDK or externally connect 1uF capacitance to ground. For the merged version of VDDK, it is actually empty; For the discrete version, it is actually AVDDK.
8	28	-	-	RSVD.	P	Reserved, it is recommended to short circuit to VDDK or externally connect 0.1uF capacitance to ground. For the merged version of VDDK, it is actually empty; For the discrete version, it is actually DVDDK.
-	-	8	9	NC.	P	Reserved, recommended suspension For the merged version of VDDK, it is actually empty;

CH390D Pin No.	CH390F Pin No.	CH390H Pin No.	CH390L Pin No.	Pin Name	Type	Pin Description
						For the discrete version, the 2# pin has actually been shorted.
-	-	9	-	NC.	P	Reserved, recommended suspension For the merged version of VDDK, it is actually empty; For the discrete version, AVDD33 is optional.
6	15	29	42	AVDD33	P	3.3V main power supply input, it is recommended to place 0.1uF parallel 10uF capacitor to ground close to the chip, or a single 1uF~4.7uF capacitor.
10	16	15	23	AVDD33	P	Optional 3.3V power input, connection is recommended, and a single 1uF or 0.1uF capacitor to ground can be selected.
6	17	21	30	VDDIO	P	The power input of I/O interface, CH390L and VDDK separate versions of CH390 support 3.3V, and VDDK combined version of CH390F/H supports 3.3V, 2.5V, 1.8V and 1.2V. It is suggested that the capacitance of 0.1 UF (0.1 UF ~ 1 UF) to ground should be placed close to the chip. *Note: VDDIO of CH390D is shorted to AVDD33 and only supports 3.3V power supply.*

CH390D Pin No.	CH390F Pin No.	CH390H Pin No.	CH390L Pin No.	Pin Name	Type	Pin Description
19	26	30	43	XI	I	Crystal oscillator input requires an external 25MHz crystal end or an external clock input.
20	27	31	44	XO	O	The inverted output of crystal oscillator needs to be externally connected to the other end of 25MHz crystal.
0	0	0/5/32	5/6/15/33/ 41/45	GND	P	Common ground.
-	-	-	47/48	GND	P	Optional ground terminal, connection is recommended.
-	-	22	-	NC.	P	Reserved, recommended suspension. For the merged version of VDDK, it is actually empty; For the discrete version, it is optional GND.
16	23	25	38	LED2ACT	O	Connect indicator LED. In LED mode 1, it is a combination LED of internal PHY link and carrier induction signal. In LED mode 0, it is only the LED of the carrier induction signal of the internal PHY.
17	24	26	39	LED1SPD	O	Speed indicator LED. Low level output indicates that the internal PHY works in 100M

CH390D Pin No.	CH390F Pin No.	CH390H Pin No.	CH390L Pin No.	Pin Name	Type	Pin Description
						mode, and floating indicates that the internal PHY works in 10M mode.
-	-	10/23	31/29	GPIO1/ GPIO2	I/O, PD	Bidirectional three-state universal input and output, default is input. Controlled by bit 1 and bit 2 of MAC registers 1Eh, 1Fh. *Note: The GPIO2 of the CH390D is internally shorted to SDI, disabling the setting of GPIO2.*
15	-	28	28	GPIO3	I/O, PD	Bidirectional three-state general-purpose inputs and outputs, defaulting to inputs. Controlled by bit 3 of MAC registers 1Eh, 1Fh.
-	-	-	22/24/25~ 29/31	D15~D8	I/O /PD	Bits 8 ~ 15 of the processor data bus Dbus are used for the 16-bit parallel port. In 16-bit mode, bits 8 to 15 as the processor data bus. In 8-bit mode, as GPIO or application-specific I/O.
			25~27	GPIO6 ~GPIO4	O/PD	In 8-bit mode, it is used as a general-purpose output. These pins can only be used as general-purpose output pins and are controlled by register 1Fh.
-	6~13	-	10~14, 16~18	D7~D0	I/O, PD	Bits 0 to 7 of the processor data bus Dbus are used for 8-bit or 16-bit parallel interfaces.
-	-	11	19	EEDIO	I/O, PD	EEPROM data input and output pins, default is low.

CH390D Pin No.	CH390F Pin No.	CH390H Pin No.	CH390L Pin No.	Pin Name	Type	Pin Description
-	-	12	20	EECK	O/PD	EEPROM clock output, default is low.
-	-	13	21	EECS	O/PD	EEPROM chip select output, active high, default is low.
-	-	-		MD8	I, PD	This pin also serves as the configuration pin for the data width of the CH390L parallel port. During power-on reset, if this pin is in 8-bit mode when pulled high by an external resistor, the data width is 8 bits. Otherwise, it is 16-bit mode with 16-bit data width.
7	14	14	22	WOL	O/PD	Network wake-up output, polarity configurable via EEPROM *Note: Not applicable to CH390L's 16-bit mode.*
11	-	17	-	SCS	I	SPI chip select input, active low.
12	-	18	-	SCK	I/PD	SPI clock input, mode 0 or 3 supported.
13	-	19	-	SDI	I/PD	SPI serial data input, connected to the MOSI of the processor SPI host.
9	-	20	-	SDO	O/PD	SPI serial data output, connected to the MISO of the processor SPI host.
14	19	24	34	INT	O	Interrupt request output, active high by default. The polarity can be set via EEPROM configuration or MAC register 39H.
18	25	27	40	RSTB	I/PU	Reset input, active low.

CH390D Pin No.	CH390F Pin No.	CH390H Pin No.	CH390L Pin No.	Pin Name	Type	Pin Description
-	18	-	32	CMD	I/PD	Parallel Interface. This cycle command type selection input. Selects access to the data port when high. When low, access to the INDEX address index port is selected
-	20	-	35	RDB	I/PD	The processor parallel port reads the control signal input. The default is active low and the polarity is configurable via EEPROM.
-	21	-	36	WRB	I/PD	Processor parallel port write control signal input. The default is active low and the polarity is configurable via EEPROM.
-	22	-	37	CSB	I/PU	Processor parallel port chip select input. The default is active low and the polarity is configurable via EEPROM.
-	-	16	46	NC.	-	Empty pins.

Note: I = Input;

O = Output;

I/O = Input/Output;

P = Power supply;

PD = Internal pull-down resistor;

PU = Internal pull-up resistor.

5. Register Description

Note: In this datasheet, (L) indicates that it applies to CH390L; (F) indicates that it applies to CH390F; (H) indicates that it applies to CH390H; (D) indicates that it applies to CH390D, or if not indicated, that it applies to CH390H, CH390D, CH390L and CH390F.

Table 5-1 Register list

Register	Description	Offset	Default value after reset
NCR	Network Control Register	00h	00h
NSR	Network Status Register	01h	00h
TCR	TX Control Register	02h	00h
TSRA	TX Status Register A	03h	00h
TSRB	TX Status Register B	04h	00h
RCR	RX Control Register	05h	00h
RSR	RX Status Register	06h	00h
ROCR	Receive Overflow Counter Register	07h	00h
BPTR	Back Pressure Threshold Register	08h	37h
FCTR	Flow Control Threshold Register	09h	38h
FCR	RX/TX Flow Control Register	0Ah	00h
EPCR	EEPROM&PHY Control Registers	0Bh	00h
EPAR	EEPROM&PHY Address Registers	0Ch	40h
EPDRL	EEPROM&PHY Low Byte Data Register	0Dh	XXh
EPDRH	EEPROM&PHY High Byte Data Register	0Eh	XXh
WCR	Wake Up Control Register	0Fh	00h
PAR	Ethernet MAC Physical Address Register	10h~15h	Built-in unique Ethernet address, configurable override by EEPROM
MAR	Multicast Address Hash Table Register	16h~1Dh	XXh
GPCR(L/H/D)	General-purpose Control Register	1Eh	71h
GPR	General-purpose Register	1Fh	XXh
TRPAL	TX Memory Read Pointer Address Low Byte	22h	00h
TRPAH	TX Memory Read Pointer Address High Byte	23h	00h
RWPAL	RX Memory Write Pointer Address Low Byte	24h	00h
RWPAH	RX Memory Write Pointer Address High Byte	25h	0Ch
VID	Vendor ID	28h~29h	1C00h
PID	Product ID	2Ah~2Bh	9151h(H/D)/9150h(L/F)
CHIPR	CHIP Revision	2Ch	2Bh(H/D)/2Ah(L/F)
TCR2	Transmit Control Register 2	2Dh	00h
ETXCSR(L/F)	Early transmission control/status register	30h	00h
ATCR(H/D)	Automatic transmission control register	30h	00h
TCSCR	Transmit Check Sum Control Registers	31h	00h
RCSCSR	Receive Check Sum Control Status	32h	00h

Register	Description	Offset	Default value after reset
	Register		
MPAR	MII PHY Address Register	33h	00h
LEDCR(L)	LED Control Register	34h	00h
SBCR(H/D)	SPI Bus Control Register	38h	44h
INTCR	INT Pin Control Register	39h	00h
ALNCR(H/D)	SPI Byte Align Error Counter Register	4Ah	00h
SCCR	System Clock Turn ON Control Register	50h	00h
RSCCR	Resume System Clock Control Register	51h	XXh
RLENCR	RX Packet Length Control Register	52h	00h
BCASTCR	RX Broadcast Control Register	53h	00h
INTCKCR(H/D)	INT Pin Clock Output Control Register	54h	00h
MPTRCR	Memory Pointer Control Register	55h	00h
MLEDCR(H/D)	More LED Control Register	57h	00h
MRCMDX	Memory Data Pre-Fetch Read Command Without Address Increment Register	70h(H/D)/F0h(L/F)	XXh
MRCMDX1	Memory Read Command Without Pre-Fetch and Without Address Increment Register	71h(H/D)/F1h(L/F)	XXh
MRCMD	Memory Data Read Command with Address Increment Register	72h(H/D)/F2h(L/F)	XXh
MRRL	Memory Data Read Address Register Low Byte	74h(H/D)/F4h(L/F)	00h
MRRH	Memory Data Read Address Register High Byte	75h(H/D)/F5h(L/F)	00h
MWCMDX	Memory Data Write Command Without Address Increment Register	76h(H/D)/F6h(L/F)	XXh
MWCMD	Memory Data Write Command Without Address Increment Register	78h(H/D)/F8h(L/F)	XXh
MWRL	Memory Data Write Address Register Low Byte	7Ah(H/D)/FAh(L/F)	00h
MWRH	Memory Data Write Address Register High Byte	7Bh(H/D)/FBh(L/F)	00h
TXPLL	TX Packet Length Low Byte Register	7Ch(H/D)/FCh(L/F)	XXh
TXPLH	TX Packet Length High Byte Register	7Dh(H/D)/FDh(L/F)	XXh
ISR	Interrupt Status Register	7Eh(H/D)/FEh(L/F)	00h
IMR	Interrupt Mask Register	7Fh(H/D)/FFh(L/F)	00h

Note: In the register description, the default form is as follows.

Reset Value:

1 Bit set to logic one

0 Bit set to logic zero

X No default value

P = Power on reset default value

H = Hardware reset default value

S = Software reset default value

Access Type:

RO = Read Only

RW = Read/Write

R/C = Read and Clear

RW/C1 = read/write, clear by write 1

WO = Write Only

E = Default value from EEPROM

T = Default value from strap pin

h = Hex, format

Reserved bits are undefined on read/write access.

5.1 Network Control Register (00h)

Bit	Name	Description	Access	Default value
7	Reserved	Reserved	RO	P0
6	WAKEEN	Enable Wakeup Function. Clearing this bit will also clear all wake-up event states, and this bit will not be affected by a software reset. 1 = Enable; 0 = Disable.	RW	P0
5	Reserved	Reserved	RO	00
4	MACPD	Write after read fetch inverse to enable wake-up frame notification.	RW	PS0
3	FDX	Duplex Mode of the Internal PHY. 1 = Full-duplex; 0 = Half-duplex. (Reserved, disable)	RO	PS0
2:1	LBK	Loopback Mode Bit: 2 1 0 0 Normal; 0 1 MAC internal loopback; 1 0 Reserved; 1 1 Reserved.	RW	PS00
0	RST	Software Reset and Auto-Clear after 10us 1 = Reset state; 0 = Non-reset state.	RW	P0

5.2 Network Status Register (01h)

Bit	Name	Description	Access	Default value
7	SPEED	Speed of Internal PHY This bit has no meaning when LINKST=0. 1 = 10Mbps; 0 = 100Mbps.	RO	X
6	LINKST	Link Status of Internal PHY 1 = Link OK; 0 = Link failed.	RO	X
5	WAKEST	Wakeup Event Status Clears by read or write 1. This bit will not be affected after software reset. 1 = Wakeup event; 0 = No wakeup event.	RW/C1	P0
4	Reserved	Reserved	RO	0
3	TX2END	TX Packet Index B Complete Status Auto-Clear at begin transmitting of TX packet index B and Auto-Set at the end of transmitting of TX packet index B. 1 = Transmit completion or idle of packet index B; 0 = Packet index B transmit in progress.	RW/C1	PS1

2	TX1END	TX Packet Index A Complete Status Auto-Clear at begin transmitting of TX packet index A and Auto-Set at the end of transmitting of TX packet index A. 1 = Transmit completion or idle of packet index A; 0 = Packet index A transmit in progress.	RW/C1	PS1
1	RXOV	RX Memory Overflow Status 1 = RX memory Overflow; 0 = Non-overflow.	RO	PS0
0	RXRDY	RX Packet Ready (H/D) 1 = Have packet in RX memory; 0 = No packet in RX memory.	RO	PS0

5.3 TX Control Register TCR (02h)

Bit	Name	Description	Access	Default value
7	Reserved	Reserved	RO	0
6	TJDIS	Transmit Jabber Timer (2048 bytes) Control 1 = Disabled; 0 = Enable.	RW	PS0
5	Reserved	Reserved	RO	0
4	PAD_DIS2	PAD Appends for Packet Index B 1 = Disable; 0 = Enable.	RW	PS0
3	CRC_DIS2	CRC Appends for Packet Index B 1 = Disable; 0 = Enable.	RW	PS0
2	PAD_DIS1	PAD Appends for Packet Index A 1 = Disable; 0 = Enable.	RW	PS0
1	CRC_DIS1	CRC Appends for Packet Index A 1 = Disable; 0 = Enable.	RW	PS0
0	TXREQ	TX Request. Auto-Clear after Sending Completely 1 = Transmit in progress; 0 = No transmit in progress.	RW	PS0

5.4 TX Status Register TSRA for Packet Index A(03h)

Bit	Name	Description	Access	Default value
7	TJTO	Transmit Jabber Time Out It is set to indicate that the transmitted frame is truncated due to more than 2048 bytes are transmitted. 1 = Timeout; 0 = Non-timeout.	RO	PS0
6	LC	Loss of Carrier It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode. 1 = Loss of carrier; 0 = No carrier have been loss.	RO	PS0
5	NC	No Carrier It is set to indicate that there is no carrier signal during the frame transmission. It is not valid in internal loopback mode. 1 = No carrier during transmit; 0 = Normal carrier status during transmit.	RO	PS0

4	LCOL	Late Collision It is set when a collision occurs after the collision window of 64 bytes. 1 = Late collision; 0 = No late collision.	RO	PS0
3	COL	Collision Packet It is set to indicate that the collision occurs during transmission. 1 = Have been collision; 0 = No collision.	RO	PS0
2	EC	Excessive Collision It is set to indicate that the transmission is aborted due to 16 excessive collisions. 1 = 16 excessive collisions; 0 = Less than 16 collisions.	RO	PS0
1:0	Reserved	Reserved	RO	0

5.5 TX Status Register TSRB for Packet Index B(04h)

Bit	Name	Description	Access	Default value
7	TJTO	Transmit Jabber Time Out It is set to indicate that the transmitted frame is truncated due to more than 2048 bytes are transmitted. 1 = Timeout; 0 = Non-timeout.	RO	PS0
6	LC	Loss of Carrier It is set to indicate the loss of carrier during the frame transmission. It is not valid in internal loopback mode. 1 = Loss of carrier; 0 = No carrier have been loss.	RO	PS0
5	NC	No Carrier It is set to indicate that there is no carrier signal during the frame transmission. It is not valid in internal loopback mode. 1 = No carrier during transmit; 0 = Normal carrier status during transmit.	RO	PS0
4	LCOL	Late Collision It is set when a collision occurs after the collision window of 64 bytes. 1 = Late collision; 0 = No late collision.	RO	PS0
3	COL	Collision Packet It is set to indicate that the collision occurs during transmission. 1 = Have been collision; 0 = No collision.	RO	PS0
2	EC	Excessive Collision It is set to indicate that the transmission is aborted due to 16 excessive collisions. 1 = 16 excessive collisions; 0 = Less than 16 collisions.	RO	PS0
1:0	Reserved	Reserved	RO	0

5.6 RX Control Register RCR (05h)

Bit	Name	Description	Access	Default value
7	Reserved	Reserved	RW	PS0
6	WTDIS	Watchdog Timer Disable 1 = When set, the Watchdog Timer (2048 bytes) is disabled; 0 = Otherwise it is enabled.	RW	PS0
5	Reserved	Reserved	RO	PS0
4	DIS_CRC	Discard CRC Error Packet 1 = Enable; 0 = Disable.	RW	PS0
3	ALL	Receive All Multicast To receive packet with multicast destination address 1 = Enable; 0 = Disable.	RW	PS0
2	RUNT	Receive Runt Packet To receive packet with size less than 64-bytes 1 = Enable; 0 = Disable.	RW	PS0
1	PRMSC	Promiscuous Mode To receive packet without destination address checking 1 = Enable; 0 = Disable.	RW	PS0
0	RXEN	RX Enable 1 = Enable; 0 = Disable.	RW	PS0

5.7 RX Status Register RSR (06h)

Bit	Name	Description	Access	Default value
7	RF	Runt Frame It is set to indicate that the size of the received frame is smaller than 64 bytes. 1 = Affirmative; 0 = Negative.	RO	PS0
6	MF	Multicast Frame It is set to indicate that the received frame has a multicast address. 1 = Affirmative; 0 = Negative.	RO	PS0
5	LCS	Late Collision Seen It is set to indicate that a late collision is found during the frame reception. 1 = Affirmative; 0 = Negative.	RO	PS0
4	RWTO	Receive Watchdog Time-Out It is set to indicate that it receives more than 2048 bytes. 1 = Affirmative; 0 = Negative.	RO	PS0
3	PLE	Physical Layer Error It is set to indicate that a physical layer error is found during the frame reception. 1 = Affirmative; 0 = Negative.	RO	PS0
2	AE	Alignment Error It is set to indicate that the received frame ends with a	RO	PS0

		non-byte aligned. 1 = Affirmative; 0 = Negative.		
1	CE	CRC Error It is set to indicate that the received frame ends with a CRC error. 1 = Affirmative; 0 = Negative.	RO	PS0
0	FOE	RX Memory Overflow Error It is set to indicate that a RX memory overflow error happens during the frame reception. 1 = Affirmative; 0 = Negative.	RO	PS0

5.8 Receive Overflow Counter Register ROCR (07h)

Bit	Name	Description	Access	Default value
7	RXFU	Receive Overflow Counter Overflow This bit is set when the ROC has an overflow condition. 1 = Affirmative; 0 = Negative.	R/C	PS0
6:0	ROC	Receive Overflow Counter Add 1 to every two packets and count the counter, which is used to display the amount of packets received when FIFO overflows.	R/C	PS0

5.9 Back Pressure Threshold Register BPTR (08h)

Bit	Name	Description	Access	Default value
7:4	BPHW	Back Pressure High Water Overflow Threshold MAC will generate the jam pattern when RX SRAM free space is lower than this threshold value. The default is 3K-byte free space. *Note: Do not exceed SRAM size.*	RW	PS3
3:0	Reserved	Reserved	RO	0

5.10 Flow Control Threshold Register FCTR (09h)

Bit	Name	Description	Access	Default value
7:4	HWOT	RX Memory High Water Overflow Threshold Send a pause packet with pause time=FFFFH when the RX memory free space is less than this value. If this value is zero, it means no RX flow control. The default value is 3K-byte free space. *Note: Do not exceed SRAM size.*	RW	PS3
3:0	LWOT	RX Memory Low Water Overflow Threshold Send a pause packet with pause time=0000H when RX memory free space is larger than this value. This pause packet is enabled after the high water pause packet is transmitted. The default memory free space is 8K-byte. *Note: Do not exceed SRAM size.*	RW	PS8

5.11 RX/TX Flow Control Register FCR (0Ah)

Bit	Name	Description	Access	Default value
7	TXP0	Force TX Pause Packet with 0000H Set to TX pause packet with pause time field is 0000H. Auto-Clears after pause packet transmission completion.	RW	PS0
6	TXPF	Force TX Pause Packet with FFFFH Set to TX pause packet with pause time field is FFFFH. Auto-Clears after pause packet transmission completion.	RW	PS0
5	TXPEN	TX Pause Packet Enable Enables the pause packet for high/low water threshold control in Full-Duplex mode. 1 = Enable; 0 = Disable.	RW	PS0
4	BKPA	Back Pressure Mode This mode is for Half-Duplex mode only. It generates a jam pattern when any packet comes and RX SRAM is over BPHW of MAC register 8H. 1 = Enable; 0 = Disable	RW	PS0
3	BKPM	Back Pressure Mode This mode is for Half-Duplex mode only. It generates a jam pattern when a packet's DA matches and RX SRAM is over BPHW of MAC register 8H. 1 = Enable; 0 = Disable.	RW	PS0
2	RXPS	RX Pause Packet Status, Latch and Read Clearly When there has been packet received, this bit will be latched. This bit is cleared after read. 1 = Has been receive pause packet; 0 = No pause packet received.	R/C	PS0
1	RXPCS	RX Pause Packet Current Status 1 = Received pause packet timer down-count in progress; 0 = Pause packet timer value is zero.	RO	PS0
0	FLCE	Flow Control Enable 1 = Enable; 0 = Disable	RW	PS0

5.12 EEPROM & PHY Control Register EPCR(0Bh)

Bit	Name	Description	Access	Default value
7:6	Reserved	Reserved	RO	0
5	REEP	Reload EEPROM (H/L) Set one to reload EEPROM. Driver needs to clear it before to enable this function.	RW	P0
4	Reserved	Reserved	RW	P0
3	EPOS	EEPROM or PHY Operation Select 0 = Select EEPROM; 1 = Select PHY. *Note: The current version only supports PHY, selecting EEPROM is not yet implemented.*	RW	P0

2	ERPRR	EEPROM Read or PHY Register Read Command Set 1 to read EEPROM or PHY register.	RW	P0
1	ERPRW	EEPROM Write or PHY Register Write Command Set 1 to write EEPROM or PHY register.	RW	P0
0	ERRE	EEPROM Access Status or PHY Access Status 1 = The EEPROM or PHY access is in progress 0 = Completion of the EEPROM or PHY access	RO	P0

5.13 EEPROM & PHY Address Register EPAR (0Ch)

Bit	Name	Description	Access	Default value
7:6	PHY_ADR	PHY Address bit 1 and 0, the PHY address bit [4:2] is force to 0. Force to 01 in application.	RW	P01
5:0	EROA	EEPROM Word Address or PHY Register Number.	RW	P0

5.14 EEPROM & PHY Data Register EPDRL/EPDRH (EE_PHY_L:0Dh, EE_PHY_H:0Eh)

Bit	Name	Description	Access	Default value
7:0	EPDRL EE_PHY_L	EEPROM or PHY Low Byte Data The low byte data read from or write to EEPROM or PHY.	RW	P0
7:0	EPDRH EE_PHY_H	EEPROM or PHY High Byte Data The high byte data read from or write to EEPROM or PHY.	RW	P0

5.15 Wake Up Control Register WCR (0Fh)

Bit	Name	Description	Access	Default value
7:6	Reserved	Reserved	RO	0
5	LINKEN	Link Status Change Wake up Event To control the link status change event in WOL pin function. This bit will not be affected after software reset. 1 = Enable; 0 = Disable.	RW	P0
4	SAMPLEEN	Sample Frame Wake up Event Enable To control the sample frame matched event in WOL pin function. This bit will not be affected after software reset. 1 = Enable; 0 = Disable *Note: It is not recommended to enable MAGICEN to wake up through magic package.*	RW	P0
3	MAGICEN	Magic Packet Wake up Event To control the Magic packet event in WOL pin function. This bit will not be affected after software reset. 1 = Enable; 0 = Disable	RW	P0
2	LINKST	Link Status Change Event Occurred 1 = Link change event occurred; 0 = No link change event.	RO	P0

1	SAMPLEST	Sample Frame Event Occurred 1 = Sample frame matched event occurred; 0 = No sample frame matched.	RO	P0
0	MAGICST	Magic Packet Event Occurred 1 = Magic packet received; 0 = No magic packet received.	RO	P0

Note: For CH390L, this register only applies to 8-bit mode.

5.16 Ethernet MAC Physical Address Register PAR0~PAR5 (PAB0~PAB5:10h~15h)

Bit	Name	Description	Access	Default value
7:0	PAR5	Physical Address Byte 5 (15h)	RW	E
7:0	PAR4	Physical Address Byte 4 (14h)	RW	E
7:0	PAR3	Physical Address Byte 3 (13h)	RW	E
7:0	PAR2	Physical Address Byte 2 (12h)	RW	E
7:0	PAR1	Physical Address Byte 1 (11h)	RW	E
7:0	PAR0	Physical Address Byte 0 (10h)	RW	E

Note: Each chip has a unique Ethernet MAC address built in and will replace this built-in address if the EEPROM configuration data is valid.

5.17 Ethernet MAC Physical Address Register MAR0~MAR7(MAB0~MAB5:16h~1Dh)

Bit	Name	Description	Access	Default value
7:0	MAR7	Multicast Address Hash Table Byte 7 (1Dh)	RW	X
7:0	MAR6	Multicast Address Hash Table Byte 6 (1Ch)	RW	X
7:0	MAR5	Multicast Address Hash Table Byte 5 (1Bh)	RW	X
7:0	MAR4	Multicast Address Hash Table Byte 4 (1Ah)	RW	X
7:0	MAR3	Multicast Address Hash Table Byte 3 (19h)	RW	X
7:0	MAR2	Multicast Address Hash Table Byte 2 (18h)	RW	X
7:0	MAR1	Multicast Address Hash Table Byte 1 (17h)	RW	X
7:0	MAR0	Multicast Address Hash Table Byte 0 (16h)	RW	X

5.18 General-purpose Control Register (L/H/D) GPCR (1Eh)

Bit	Name	Description	Access	Default value
7	Reserved	Reserved	RO	PH0
6:4	GPC64	Define the input/output direction of pin GPIO6~4. (L) These bits are forced to "1" and pins GPIO6 to 4 can only be output.	RO	P111
3	GPC3	Define the input/output direction of pin GPIO3. (L/H/D) 1 = Pin GPIO3 in output mode; 0 = Pin GPIO3 in input mode.	RW	P0
2	GPC2	Define the input/output direction of pin GPIO2. (L/H) 1 = Pin GPIO2 in output mode; 0 = Pin GPIO3 in input mode. *Note: The CH390D's GPIO2 is internally shorted to SDI, disabling the setting of this bit to 1.*	RW	P0
1	GPC1	Define the input/output direction of pin GPIO1. (L/H) 1 = Pin GPIO1 in output mode;	RW	P0

		0 = Pin GPIO1 in input mode.		
0	Reserved	Reserved	RO	P1

Note: For CH390L, this register only applies to 8-bit mode.

5.19 General-purpose Register (1Fh)

Bit	Name	Description	Access	Default value
7	Reserved	Reserved	RO	0
6:4	GPO	The output data of GPIO6 ~ 4. (L) These bits are output to pins GPIO6~4, respectively.	RW	P0
3	GPIO3	Output data or input status of GPIO3. (L/H/D) When GPC3 of register 1EH is 1, the value of this bit is reflected to pin GP3. When GPC3 of register 1EH is 0, the value of this bit to be read is reflected from correspondent pin of GP3.	RW	P0
2	GPIO2	Output data or input status of GPIO2. (L/H) When GPC2 of register 1EH is 1, the value of this bit is reflected to pin GPIO2. When GPC2 of register 1EH is 0, the value of this bit to be read is reflected from correspondent pin of GPIO2.	RW	P0
1	GPIO1	Output data or input status of GPIO1. (L/H) When GPC1 of register 1EH is 1, the value of this bit is reflected to pin GPIO1. When GPC1 of register 1EH is 0, the value of this bit to be read is reflected from correspondent pin of GPIO1.	RW	P0
0	PHYPD	PHY Power Down Control, Sleep mode setting. 1 = Power down PHY; 0 = Power up PHY. In Sleep mode, power off the PHY but keep the system clock module on. *Note: If restarting PHY power, it is recommended to access CH390 after 100us.*	RW	PE1

Note: For CH390L, bits 1 to 6 in this register apply only to 8-bit mode.

5.20 TX Memory Read Pointer Address Register TRPAL/TRPAH(22h~23h)

Bit	Name	Description	Access	Default value
7:0	TRPAH	TX Memory Read Pointer Address High Byte (23h)	RO	PS0
7:0	TRPAL	TX Memory Read Pointer Address Low Byte (22h)	RO	PS0

5.21 RX Memory Write Pointer Address Register RWPAL/RWPAH(24h~25h)

Bit	Name	Description	Access	Default value
7:0	RWPAH	RX Memory Write Pointer Address High Byte (25h)	RO	PS,0Ch
7:0	RWPAL	RX Memory Write Pointer Address Low Byte (24h)	RO	PS,00h

5.22 Vendor ID Register VIDL/VIDH (28h~29h)

Bit	Name	Description	Access	Default value
7:0	VIDH	Vendor ID High Byte (29h)	RO	PE,1Ch
7:0	VIDL	Vendor ID Low Byte (28h)	RO	PE,00h

5.23 Product ID Register PIDL/PIDH (2Ah~2Bh)

Bit	Name	Description	Access	Default value
7:0	PIDH	Product ID High Byte (2Bh)	RO	PE,91h
7:0	PIDL	Product ID Low Byte (2Ah)	RO	PE,51h(H/D)/ 50h(L/F)

5.24 Chip revision identification code CHIPR (2Ch)

Bit	Name	Description	Access	Default value
7:0	CHIPR	CHIP Revision	RO	P,2Bh(H/D) /2Ah(L/F)

5.25 Transmit control register 2 TCR2 (2Dh)

Bit	Name	Description	Access	Default value
7	LED	LED Mode 1 = LED mode 1; 0 = LED mode 0. The default is mode 0, which can be configured via EEPROM. *Note: For CH390H/D, more configurations can be found in register 57h.*	RW	PE0
6	RLCP	Retry Late Collision Packet Re-transmit the packet with late-collision. 1 = Enable; 0 = Disable.	RW	P0
5:4	Reserved	Reserved	RW	P0
3:0	IFGS	Inter-Frame Gap Setting 0XXX = 96-bit; 1000 = 64-bit; 1001 = 72-bit; 1010 = 80-bit; 1011 = 88-bit; 1100 = 96-bit; 1101 = 104-bit; 1110 = 112-bit; 1111 = 120-bit.	RW	P00

5.26 Early Transmit Control/Status Register (L/F) ETXCSR (30h)

Bit	Name	Description	Access	Default value
7	ETE	Early Transmit Enable 1: Enable bits [2:0]; 0: DISABLE.	RW	PS0
6	Reserved	Reserved	RO	PS0

<table>
<tr><td>5</td><td>Reserved</td><td>Reserved</td><td>RO</td><td>PS0</td></tr>
<tr><td>4:2</td><td>Reserved</td><td>Reserved</td><td>RO</td><td>000</td></tr>
<tr><td>1:0</td><td>ETT</td><td>Early Transmit Threshold
Start transmit when data write to TX FIFO reach the byte-count threshold.
Note: It is necessary to ensure the data writing speed of the parallel port, otherwise the data is insufficient.
<table><tr><th>Bit-1</th><th>Bit-0</th><th>Threshold</th></tr><tr><td>0</td><td>0</td><td>12.5%</td></tr><tr><td>0</td><td>1</td><td>25%</td></tr><tr><td>1</td><td>0</td><td>50%</td></tr><tr><td>1</td><td>1</td><td>75%</td></tr></table></td><td>RW</td><td>PS0</td></tr>
</table>

5.27 Auto-Transmit Control Register (H/D) ATCR (30h)

Bit	Name	Description	Access	Default value
7	AUTO_TX	Auto-Transmit Control 1 = Auto-Transmit enabled. Auto-transmission when TX data writing is finished. 0 = Auto-Transmit disabled. When transmit packet, need to set MAC register 2H bit 0 to “1”	RW	PS0
6:2	Reserved	Reserved	RO	P00
1:0	Reserved	Reserved	RW	PS0

5.28 Transmit Check Sum Control Register TCSCR (31h)

Bit	Name	Description	Access	Default value
7:5	Reserved	Reserved	RO	0
4	IPv6TCPCSE	IPv6 TCP CheckSum Generation 1 = Enable; 0 = Disable.	RW	PS0
3	IPv6UDPCSE	IPv6 UDP CheckSum Generation 1 = Enable; 0 = Disable.	RW	PS0
2	UDPCSE	UDP CheckSum Generation 1 = Enable; 0 = Disable.	RW	PS0
1	TCPCSE	TCP CheckSum Generation 1 = Enable; 0 = Disable.	RW	PS0
0	IPCSE	IP CheckSum Generation 1 = Enable; 0 = Disable. *Note: One of UDPCSE or TCPCSE needs to be enabled at the same time.*	RW	PS0

5.29 Receive Check Sum Status Register RCSCSR (32h)

Bit	Name	Description	Access	Default value
7	UDPS	UDP CheckSum Status 1 = Checksum fail; 0 = No UDP checksum error.	RO	PS0
6	TCPS	TCP CheckSum Status	RO	PS0

		1 = Checksum fail; 0 = No TCP checksum error.		
5	IPS	IP CheckSum Status 1 = Checksum fail; 0 = No IP checksum error.	RO	PS0
4	UDPP	UDP Packet of Current Received Packet 1 = UDP packet; 0 = Non UDP packet.	RO	PS0
3	TCPP	TCP Packet of Current Received Packet 1 = TCP packet; 0 = Non TCP packet.	RO	PS0
2	IPP	IP Packet of Current Received Packet 1 = IP packet; 0 = Non IP packet.	RO	PS0
1	RCSEN	Receive CheckSum Checking Enable When set, the checksum status (bit 7~2) will be stored in bit 7:2 of packet's first byte of RX packets status header respectively. 1 = Enable; 0 = Disable.	RW	PS0
0	DCSE	Discard CheckSum Error Packet When set, if IPv4/TCP/UDP checksum field is error, this packet will be discarded. 1 = Enable; 0 = Disable.	RW	PS0

5.30 MII PHY Address Register MPAR (33h)

Bit	Name	Description	Access	Default value
7	ADR_EN	Redefine PHY Address 1: Enable; 0: Disable.	RW	HPS0
6:5	Reserved	Reserved	RO	HPS0
4:0	EPHYADR	Redefined PHY Address Bit 4~0.	RW	HPS01

5.31 LED Pin Control Register (L) LEDCR (34h)

Bit	Name	Description	Access	Default value
7:2	Reserved	Reserved	RO	PS0
1	GPIO	LED act as General-purpose signals in 16-bit mode 1: Pin 38/39 (LED2/1) act as the general-purpose pins that are controlled by registers 1Eh bit 2/1 and 1Fh bit 2/1 respectively. 0: Disable.	RW	P0
0	MII	LED act as SMI signals in 16-bit mode 1: Pin 38/39 (LED2/1) act as the MII Management Interface mode. In this mode, the LED1 act as data (MDIO) signal and the LED2 act as sourced clock (MDC) signal. These two-pin are controlled by registers 0Bh,0Ch, and 0Dh. 0: Disable.	RW	P0

5.32 SPI Bus Control Register (H/D) SBCR (38h)

Bit	Name	Description	Access	Default value
7:5	Reserved	Reserved	RO	P0
4:3	Reserved	Reserved	RO	P00
2	SCS_SPIKE	Eliminate SPI_CSB Spike	RW	PE1

		1 = Eliminate about 2ns SPI_CSB spike		
1:0	Reserved	Reserved	RO	P00

5.33 INT Pin Control Register INTCR (39h)

Bit	Name	Description	Access	Default value
7:2	Reserved	Reserved	RO	PS0
1	INT_TYPE	INT Pin Output Type Control 1 = INT Open-drain output; 0 = INT push-pull output.	RW	PET0
0	INT_POL	INT Pin Polarity Control 1 = INT active low; 0 = INT active high.	RW	PET0

5.34 SPI Byte Align Error Counter Register (H/D) ALNCR (4Ah)

Bit	Name	Description	Access	Default value
7:0	ALN_ERR	SPI Clock Byte Align Error Counter The counter to count the byte align error of SCK at end of CSN. The maximum value is 255. Write any value to clear 0.	RO	P00

5.35 System Clock Turn ON Control Register SCCR(50h)

Bit	Name	Description	Access	Default value
7:1	Reserved	Reserved	RO	0
0	DIS_CLK	Stop Internal System Clock, Stop mode setting. 1 = Entering shutdown mode, with the system clock off and the internal PHY powered down; 0 = Non-shutdown mode, system clock on. Refer to register 51h.	W	P0

5.36 Resume System Clock Control Register RSCCR (51h)

When the INDEX port set to 51H, it will exit the Stop mode, and the internal system clock is turn ON. It is recommended to access CH390 after 2ms.

5.37 RX Packet Length Control Register RLENCR (52h)

Bit	Name	Description	Access	Default value
7	RXLEN	RX packet length filter. 1 = Enable RX packet length filter; 0 = Not enable RX packet length filter.	RW	PS0
6:5	Reserved	Reserved	RO	P00
4:0	MAXRXLEN	Maximum RX Packet Length Allowed (unit 64-byte) If the data length exceeds the (MAXRXLEN*64+1) count, the RX packet is discarded. *Note: All bits 0 means no length limitation.*	RW	PS0

5.38 RX Broadcast Control Register BCASTCR (53h)

Bit	Name	Description	Access	Default value

7:6	BC_EN	New RX Broadcast Packet Control Mode 0X = Broadcast packets controlled by bit 7 of MAC register 1Dh; 10 = Broadcast packets are not received (Hashing packets that conform to the rules are not affected); 11 = Enable packet length filter of broadcast packet.	RW	PS0
5	Reserved	Reserved	RO	P0
4:0	MAXBCLEN	Maximum RX Broadcast Packet Length Allowed (unit 64-byte) The RX packet will be discarded if the data length is more than (MAXBCLEN*64+1) count. *Note: All bits 0 means no length limitation.*	RW	PS0

5.39 INT Pin Clock Output Control Register INTCKCR (H/D) INTCKCR (54h)

Bit	Name	Description	Access	Default value
7	INT_CTL	Select Control Method for INT Pin 1 = Enable INT pin in this register; 0 = INT pin output controlled by MAC register 39H.	RW	PS0
6	CK_UNIT	Select Clock Output Duty Cycle Width Unit 1 = 2.6ms; 0 = 40.96us.	RW	PS0
5	Reserved	Reserved	RO	P0
4:0	DUTY_LEN	Clock Output Duty Cycle Width *Note: All bits 0 means INT pin is controlled by register 39H.*	RW	PS0

5.40 Memory Pointer Control Register MPTRCR (55h)

Bit	Name	Description	Access	Default value
7:2	Reserved	Reserved	RO	P00
1	RST_TX	Reset TX Memory Pointer 1 = Reset TX write/read memory address, Auto-Cleared after 1us	RW	PS0
0	RST_RX	Reset RX Memory Pointer 1 = Reset RX write/read memory address, Auto-Cleared after 1us	RW	PS0

5.41 More LED Control Register (H/D) MLEDCR (57h)

Bit	Name	Description	Access	Default value
7	LED_MOD3	New LED Mode 1 = LED types in bit 2:0; 0 = The old LED mode 0 or 1 function.	RW	P0
6:3	Reserved	Reserved	RO	P00
2	LED_POL	The Reverse Polarity of LED Type 1 = LED in high active; 0 = LED in low active.	RW	P0
1:0	LED_TYPE	LED Type *Note: See following table.*	RW	P00

LED Type	LED2ACT	LED1SPD

00	Link	Traffic
01	Link & Traffic	Speed100M
10	Traffic	Speed100M
11	Link	Traffic100M

5.42 Memory Data Pre-Fetch Read Command without Address Increment Register MRCMDX (70h(H/D)/F0h(L/F))

Bit	Name	Description	Access	Default value
7:0	MRCMDX	Memory Read Command Read data from RX SRAM. After the read of this command, the read pointer of internal SRAM is unchanged. And the CH390 starts to pre-fetch the SRAM data to internal data buffers.	RO	X

5.43 Memory Data Read Command without Address Increment Register MRCMDX1 (71h(H/D)/F1h(L/F))

Bit	Name	Description	Access	Default value
7:0	MRCMDX1	Memory Read Command Read data from RX SRAM. After the read of this command, the read pointer of internal SRAM is unchanged. CH390 does not pre-fetch memory data.	RO	X

5.44 Memory Data Read Command with Address Increment Register MRCMD (72h(H/D)/F2h(L/F))

Bit	Name	Description	Access	Default value
7:0	MRCMD	Memory Read Command Read data from RX SRAM. After executing this command, add 1 to the read pointer for CH390H/D and CH390L in 8-bit mode, and add 2 to the read pointer for CH390L in 16-bit mode.	RO	X

5.45 Memory Data Read address Register MRRL/MRRH (74h~75h(H/D)/F4h~F5h(L/F))

Bit	Name	Description	Access	Default value
7:0	MDRAH	Memory Data Read_ addresses High Byte. It will be set to 0Ch, when IMR bit7 =1 (75h)	RW	PS0
7:0	MDRAL	Memory Data Read_ address Low Byte. (74h)	RW	PS0

5.46 Memory Data Write Command without Address Increment Register MWCMDX (76h(H/D)/F6h(L/F))

Bit	Name	Description	Access	Default value
7:0	MWCMDX	Write data to TX SRAM. After the write of this command, the write pointer is unchanged	WO	X

5.47 Memory Data Write Command with Address Increment Register MWCMD (78h(H/D)/F8h(L/F))

Bit	Name	Description	Access	Default value
7:0	MWCMD	Write Data to TX SRAM After executing this command, for CH390H/D and CH390L in 8-bit mode, the write pointer is added by 1; for CH390L in 16-bit mode, the write pointer is added by 2.	WO	X

5.48 Memory Data Write Address Register MWRL/MWRH (7Ah~7Bh(H/D)/FAh~FBh(L/F))

Bit	Name	Description	Access	Default value
7:0	MDWAH	Memory Data Write_ address High Byte. (7Bh)	RW	PS0
7:0	MDWAL	Memory Data Write_ address Low Byte. (7Ah)	RW	PS0

5.49 TX Packet Length Register TXPLL/TXPLH (7Ch~7Dh(H/D)/FCh~FDh(L/F))

Bit	Name	Description	Access	Default value
7:0	TXPLH	TX Packet Length High byte. (7Dh)	RW	X
7:0	TXPLL	TX Packet Length Low byte. (7Ch)	RW	X

5.50 Interrupt Status Register ISR (7Eh(H/D)/FEh(L/F))

Bit	Name	Description	Access	Default value
7	IOMODE	0 = 16-bit mode 1= 8-bit mode (L/F)	RO	T0
6	Reserved	Reserved	RO	R0
5	LNKCHG	Link Status Change 1: Affirmative; 0: Negative. *Note: Each connection status change or reset generates two interrupts for connection status change. The software can delay the interrupt for 65ms before clearing it in the interrupt program.*	RW/C1	PS0
4	UDRUN	Transmit Under-run (L/F) 1: Affirmative; 0: Negative.	RW/C1	PS0
3	ROO	Receive Overflow Counter Overflow 1: Affirmative; 0: Negative.	RW/C1	PS0
2	ROS	Receive Overflow 1: Affirmative; 0: Negative.	RW/C1	PS0
1	PT	Packet Transmitted 1: Affirmative; 0: Negative.	RW/C1	PS0
0	PR	Packet Received 1: Affirmative; 0: Negative.	RW/C1	PS0

5.51 Interrupt Mask Register IMR (7Fh(H/D)/FFh(L/F))

Bit	Name	Description	Access	Default value

7	PAR	Pointer Auto-return Mode Enable the TX/RX Memory Read/Write Pointer to automatically return to the starting address when the pointer exceeds the TX/RX memory size. When this bit is set, MAC register 75h is automatically set to 0Ch if the RX memory size is 13K bytes. 1: Enable; 0: Disable.	RW	PS0
6	Reserved	Reserved	RO	R0
5	LNKCHGI	Enable Link Status Change Interrupt 1: Enable; 0: Disable.	RW	PS0
4	UDRUNI	Enable Transmit Under-run Interrupt (L/F) 1: Enable; 0: Disable.	RW	PS0
3	ROOI	Enable Receive Overflow Counter Overflow Interrupt 1: Enable; 0: Disable.	RW	PS0
2	ROI	Enable Receive Overflow Interrupt 1: Enable; 0: Disable.	RW	PS0
1	PTI	Enable Packet Transmitted Interrupt 1: Enable; 0: Disable.	RW	PS0
0	PRI	Enable Packet Received Interrupt 1: Enable; 0: Disable.	RW	PS0

6. EEPROM Format

Note: 1. The word in this table refers to two bytes, 16 bits of data.

2. Only CH390L and CH390H can read EEPROM data during power-on reset.

Name	Word	Offset	Description
MAC address	0	0~5	6 Byte Ethernet Address
Auto-load Control	3	6~7	Bit 1:0=01: Update vendor ID and product ID Bit 3:2=01: Accept setting of WORD6 [4:0] Bit 5:4=01: Reserved, recommended to set to 00; Bit 7:6=01: Reserved, recommended to set to 01; Bit 9:8=01: Reserved, recommended to set to 00; Bit 11:10=01: Accept setting of WORD7 [7]; Bit 13:12=01: Reserved, recommended to set to 00; Bit 15:14=01: Reserved, recommended to set to 00.
Vendor ID	4	8~9	2-byte vendor ID (Default: 1C00h)
Product ID	5	10~11	2-byte product ID (Default: 9151h(H/D)/9150h(L/F))
Pin control	6	12~13	CH390H: When word 3 bit [3:2] =01, these bits can control the INT pins polarity. Bit2:0: Reserved Bit3: INT pin is active low when set 1 (default 0: active high); Bit4: INT pin is open-drain (default 0: push-pull output); Bit 15:5: Reserved.
			CH390L: When word 3 bit [3:2] =01, these bits can control the CSB, WRB, RDB and INT pins polarity. Bit0: CSB pin is active high when set 0 (default 1: active low); Bit1: WRB pin is active high when set 0 (default 1: active low); Bit2: RDB pin is active high when set 0 (default 1: active low); Bit3: INT pin is active low when set 1 (default 0: active high); Bit4: INT pin is open-drain when set 1 (default 0: push-pull output); Bit 15:5: Reserved.
Wake-up mode control	7	14~15	CH390H, Accept setting except for bit 7: Bit0: WOL pin is active low when set 1 (default 0: active high); Bit1: WOL pin is in pulse mode when set 1 (default 0: level mode); Bit2: Magic wakeup event is enabled when set 1 (default 0: disable); Bit3: link change wakeup event is enabled when set 1 (default 0: disable); Bit6:4: Reserved (default 0); Bit7: LED mode 1 when set 1 (default 0: mode 0); Bit15:8: Reserved (default 0).
			CH390L, Accept setting except for bit 7: Bit0: WOL pin is active low when set 1 (default 0: active high); Bit1: WOL pin is in pulse mode when set 1 (default 0: level mode); Bit2: Magic wakeup event is enabled when set 1 (default 0: disable); Bit3: link change wakeup event is enabled when set 1 (default 0: disable);

			Bit6:4: Reserved (default 0); Bit7: LED mode 1 when set 1 (default 0: mode 0); Bit11:8: Reserved (default 0); Bit13:12: LED2ACT act as WOL when set 10 in 16-bit mode for CH390L; Bit15:14: Reserved (default 0).

7. PHY Register

Table 7-1 PHY register description

Register Name	Address	Default value
Control Register	0x00	3100h
Status Register	0x01	7849h
PHY Identifier	0x02~0x03	7371h/9011h
Auto-Negotiation Advertisement	0x04	01E1h
Auto-Negotiation Link Partner Ability	0x05	0000h
Auto-Negotiation Expansion	0x06	0004h

Note: 1. Please refer to the IEEE 802.3 specification and the CH182DS2 manual for the above registers.

2. Please refer to the manual of CH182DS2 for the extended registers.

8. Function Register

8.1 SPI Serial Interface

The CH390H and CH390D support a slave mode SPI interface where an external SPI host (from the microcontroller MCU or CPU) provides the serial clock SCK, chip select SCS, and serial input data MOSI, and the serial output data MISO is driven by the CH390. MOSI is an SPI host output that varies on the falling edge of SCK and is sampled by the SDI pin of the CH390 on the rising edge of SCK. MISO is driven by the SDO pin of CH390, varies on the falling edge of SCK, and is sampled by the SPI host on the rising edge of SCK.

One SPI operation is started on the falling edge of SCS and stopped on the rising edge of SCS. Each SCK cycle corresponds to one data bit, and the high bit comes first when transmitting, and every 8 data bits form one byte. When the SPI is idle (i.e., SCS is high), SCK is held low for SPI mode 0 and high for SPI mode 3.

SPI Command Format:

SPI	Command Phase (MOSI pin)		Data Phase (MOSI pin)
	Byte 0 [7:0]		Byte 1
	Opcode	Register Address	Register Data
Register Write	1	A6~A0	D7~D0

SPI	Command Phase (MOSI pin)		Data Phase (MOSI pin)
	Byte 0 [7:0]		Byte 1
	Opcode	Register Address	Register Data
Register Read	0	A6~A0	D7~D0
Memory Dummy Read	0	1110000	D7~D0

SPI	Command Phase (MOSI pin)		Data Phase (MOSI pin)
	Byte 0 [7:0]		Byte 1~N
	Opcode	Register Address	Register Data
Memory Dummy Read Without Pre-fetch	0	1110001	(D7~D0)*N

Note 1: N can be 1~4.

SPI	Command Phase (MOSI pin)		Data Phase (MOSI pin)
	Byte 0 [7:0]		Byte 1~N
	Opcode	Register Address	Register Data
Memory Write	1	1111000	(D7~D0)*N

SPI	Command Phase (MOSI pin)		Data Phase (MOSI pin)
	Byte 0 [7:0]		Byte 1~N
	Opcode	Register Address	Register Data

Memory Read	0	1110010	(D7~D0)*N

SPI	Command Phase (MOSI pin)		Data Phase (MOSI pin)
	Byte 0		Byte 1~N
	Opcode	Register Address	Opcode
Auto-Transmit	1	1111100	(D7~D0)*N

Note 2:

Byte 1: Transmit Length bit 7~0 of n-byte;

Byte 2: FDh;

Byte 3: Transmit Length bit 15~8 of n-byte;

Byte 4: F8h;

Byte 5~n+4: 5~n+4: n-byte transmit data.

Note 3: This command burst is used only when register 30h bit 7 is set.

8.2 Parallel Interface

The CH390L supports a 16-bit or 8-bit passive parallel bus interface, and the CH390F supports an 8-bit passive parallel bus interface, and access to the CH390L and CH390F can be selected through the chip-selectable CSB. The CSB pin is active low by default, and can be redefined through EEPROM configuration. The CSB is used to select the specified CH390 from multiple peripherals under the system bus. , CSB can be active all the time if RDB and WRB are unshared dedicated connections, e.g. CSB fixed ground saves a GPIO.

Two ports can be accessed through the host interface, an INDEX address index port and a DATA port. The INDEX port is selected when the pin CMD = 0 and the DATA port is selected when CMD = 1. The contents of the INDEX port is the register address of the DATA port. The address of this register must be stored in the INDEX port before any register can be accessed.

8.3 Direct Memory Access Control

The CH390 provides DMA capability to simplify the access of the internal memory. After the programming of the starting address of the internal memory and then issuing a dummy read/write command to load the current data to internal data buffer, the desired location of the internal memory can be accessed by the read/write command registers. After each read/write operation, the memory address will be automatically incremented according to the current data bit width (8 or 16 bits), and the data at the next location will be automatically loaded into the internal data buffer. It is noted that the data of the first access (the dummy read/write command) in a sequential burst should be ignored because that the data was the contents of the last read/write command.

The internal memory size is 16K bytes. The first location of 3K bytes is used for the data buffer of the packet transmission. The other 13K bytes are used for the buffer of the receiving packets. So in the write memory operation, when the bit 7 of IMR is set, the memory address increment will wrap to location 0 if the end of address (i.e. 3K) is reached. In a similar way, in the read memory operation, when the bit 7 of IMR is set, the memory address increment will wrap to location 0C00h if the end of address (i.e. 16K) is reached.

8.4 Packet Transmission

Two packets can be stored in the transmit buffer at the same time, indexed A and B. Their status can be read from the TSRA and TSRB registers, respectively. the CRC and PAD additional data can be controlled by the TCR register.

After system reset, the send start address is 0 and the packet index is A. When sending a packet, first write the data to the send buffer through the write command register MWCMD, then write the byte count to the TXPLL and TXPLH registers, and finally set the TCR register bit 0 to 1 to turn on packet sending. The data of the next (index B) packet can be written to the transmit buffer before the transmission of packet A is finished. After the transmission of packet A is completed, the length of packet B is written to the TXPLL and TXPLH registers and the TCR register is set to send packet B. Subsequent packets are sent in the same manner in the order of A, B, A, B... alternately.

8.5 Packet Reception

The receive buffer is a ring buffer. After system reset, the receive buffer starts at 0C00h. Each packet contains a 4-byte frame header, data field, and CRC. the format of the 4-byte frame header is: 01h, status, data length low byte, and data length high byte.

8.6 Remote Package Wake-up

Remote Packet Wakeup supports Sample Frames and Magic Packets, which are independently enabled by SAMPLEEN and MAGICEN, respectively. Sample frame wakeup requires first configuring the related registers (Table 8-1), writing the sample wakeup frame configuration template sequentially through the EEPROM and PHY control registers, refer to EEPROM and PHY control register EPCR, EEPROM and PHY address register EPAR, EEPROM and PHY data register EPDRL/EPDRH. magic packets do not need additional configuration, it is not recommended to enable sample frames for regular applications, and MAGICEN can be enabled to realize remote packet wakeup via magic packet.

The MCU enables its own wake-up interrupt function, and reads out and inverts the MACPD of the network control register NCR before the MCU sleeps and writes it again, at this time, the MAC will no longer receive new packets (ordinary packets are directly discarded), and the WOL pin generates an interrupt to wake up the MCU when it receives a sample frame or a magic packet.

If the wake-up interrupt function is used again, before the MCU sleeps, the MACPD of the network control register NCR is read out, inverted and written again, at this time, the MAC will no longer receive new packets (ordinary packets are directly discarded), and when a sample frame or a magic packet is received, the WOL pin generates an interrupt to wake up the MCU.

Table 8-1 Structure of the sample frame filtering register group for remote wakeups

Filter register 0	Byte mask register 0							
Filter register 1	Byte mask register 1							
Filter register 2	Byte mask register 2							
Filter register 3	Byte mask register 3							
Filter register 4	Reserved	Command3	Reserved	Command2	Reserved	Command 1	Reserved	Command 0
Filter register 5	Offset 3		Offset 2		Offset 1		Offset 0	
Filter register 6	Filter 1				Filter 0			
Filter register 7	Filter 3				Filter 2			

As can be seen from the above table, the four fields of byte mask register, command, offset and filter work together to determine whether a frame is a remote sample frame, and in fact, four different frames can be set to meet the requirements. 4-bit command field, the highest bit indicates what kind of frames work, 1 is valid only for multicast addresses, 0 is valid only for unicast addresses; the second and first bits of the command

field are reserved, and bit 0 is the enable bit; offset field indicates how many bytes are offset from the frame header to start calculating the CRC16 value, the minimum is 12, and the actual effective value of this field is plus one. Bit 0 is the enable bit, set high to enable this group of filters; Offset field indicates how many bytes are offset from the frame header to start calculating the value of CRC16, the minimum fill in 12, the actual effective value of this field plus one, such as if the offset field is 1, it is the 13th byte from the beginning to start calculating the value of CRC16, that is, it is just the beginning of the first byte for the network layer. 32 byte masking indicates that the value of CRC16 is the first 31 bytes from the beginning of the definition of offset field, which needs to be set to 1, and which needs to be set to 1, and which needs to be set to 1. The 32-bit byte mask indicates the 31 bytes from the beginning of the offset field, which need to be involved in the CRC16 calculation, the highest bit of the byte mask register must be 0, and up to 31 bytes are all involved in the calculation. The filter field stores the value of the CRC result that the user expects to calculate. The MAC will compare the value of the CRC16 calculated by itself with the value in this field, and if it is the same, then the current frame passes the filter of the Remote Sample Frame Filter, and is recognized by the MAC as a Remote Wakeup Frame.

9. Electrical Characteristics

9.1 Absolute Maximum Ratings

(critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Table 9-1 Absolute maximum value parameter table

Symbol	Parameter	Min.	Max.	Unit
AVDD33	Supply Voltage	-0.4	4.0	V
VDDIO	Interface I/O pin power supply voltage	-0.4	4.0	V
V_{DDIO}	Voltage on control interface pins (VDDIO power supply)	-0.4	VDDIO+0.4	V
V_{IOX}	Voltage on Ethernet pins (AVDD33 power supply)	-0.4	AVDD33+0.4	V
T_A	Ambient Temperature	-40	+85	℃
T_s	Storage Temperature Range	-65	+150	℃
V_{ESD}	HBM ESD tolerant voltage for external pins	6		KV

9.2 Supply Current Characteristics

Table 9-2 Current consumption table (AVDD33 = 3.3V, VDDIO = 3.3V, TA = 25°C)

Symbol	Parameter	Condition	Typ.		Unit
			390H/D	390L/F	
I_{DD}	100BASE-TX	Full load transmission state	57	58	mA
		Idle status	57	57	
	10BASE-T	Full load transmission state	54	55	mA
		Idle status	26	26	
	Sleep Mode	PHY power off, system clock on	5.4	5.6	mA
	Stop Mode	PHY power off, system clock off	0.25	0.25	

9.3 Operating Voltage and DC Characteristics

Table 9-3 DC characteristics parameter table (AVDD33 = 3.3V, VDDIO = 3.3V, TA = 25°C)

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
AVDD33	Supply Voltage	AVDD33 pins	3.2	3.3	3.45	V
VDDIO	Interface I/O pin supply voltage	CH390L	2.5	3.3	3.5	V
		CH390F/H	1.1	3.3	3.5	V
		CH390D	3.1	3.3	3.5	V
V_{IL}	Input Low Voltage	VDDIO = 3.3V	0		0.8	V
		VDDIO = 1.8V	0		0.5	V
		VDDIO = 1.2V	0		0.3	V
V_{IH}	Input High Voltage	VDDIO = 3.3V	2.0		VDDIO	V
		VDDIO = 1.8V	1.2		VDDIO	V
		VDDIO = 1.2V	0.9		VDDIO	V
I_{IL}	Input Low Level Leakage Current	Input voltage 0V	-5		5	uA
I_{IH}	Input High Level Leakage Current	Input voltage	-5		5	uA

		VDDIO				
V_{OL}	Output Low Voltage	IOL = 8mA, VDDIO = 3.3V			0.4	V
		IOL = 4mA, VDDIO = 1.8V			0.4	V
		IOL = 2mA, VDDIO = 1.2V			0.3	V
V_{OH}	Output High Voltage	IOH = -8mA, VDDIO = 3.3V	VDDIO-0.4			V
		IOH = -4mA, VDDIO = 1.8V	VDDIO-0.4			V
		IOL = -2mA, VDDIO = 1.2V	VDDIO-0.3			V
Rpu	Resistance Value of the Built-in Pull-up Resistor		35	60	100	KΩ
Rpd	Resistance Value of the Built-in Pull-down Resistor		35	60	100	KΩ
V_{ICM}	RX+/RX- Common Mode Input Voltage	100Ω input impedance		1.65		V
V_{TD100}	100TX+/- Differential Output Voltage	Peak to peak		2.0		V
V_{TD10}	10TX+/- Differential Output Voltage	Peak to peak		4.6		V
V_{LVR}	Voltage threshold for power supply low voltage reset		2.6	2.9	3.1	V

9.4 DC Electrical Characteristics

9.4.1 SPI Timing

Figure 9-1 SPI M0 mode timing diagram

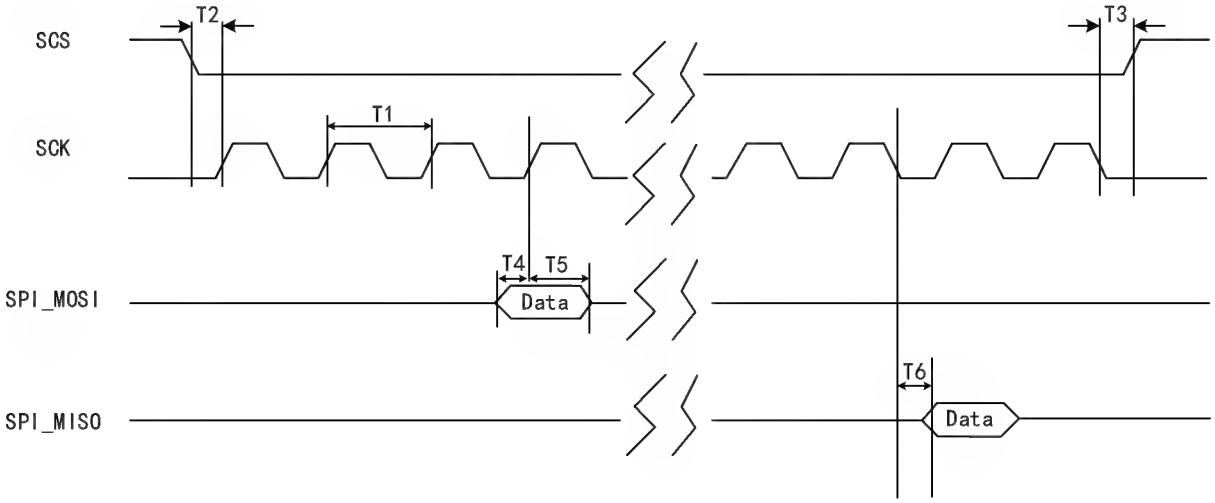


Table 9-4 SPI M0 mode parameter table (AVDD33 = 3.3V, VDDIO = 3.3V, TA = 25°C)

Symbol	Parameter		Min.	Typ.	Max.	Unit
T1	SCK Frequency	VDDIO = 3.3V		50	72	MHz

		VDDIO = 1.8V			64	MHz
		VDDIO = 1.2V			36	MHz
T2	SCS falling edge to SCK rising edge		6.5			ns
T3	SCK falling edge to SCS rising edge		6.5			ns
T4	SDI/MOSI build-up time before SCK rising edge		3			ns
T5	SDI/MOSI hold time after SCK rising edge		2			ns
T6	SDO/MISO output delay after SCK falling edge		2		6.5	ns

Figure 9-2 SPI M3 mode timing diagram

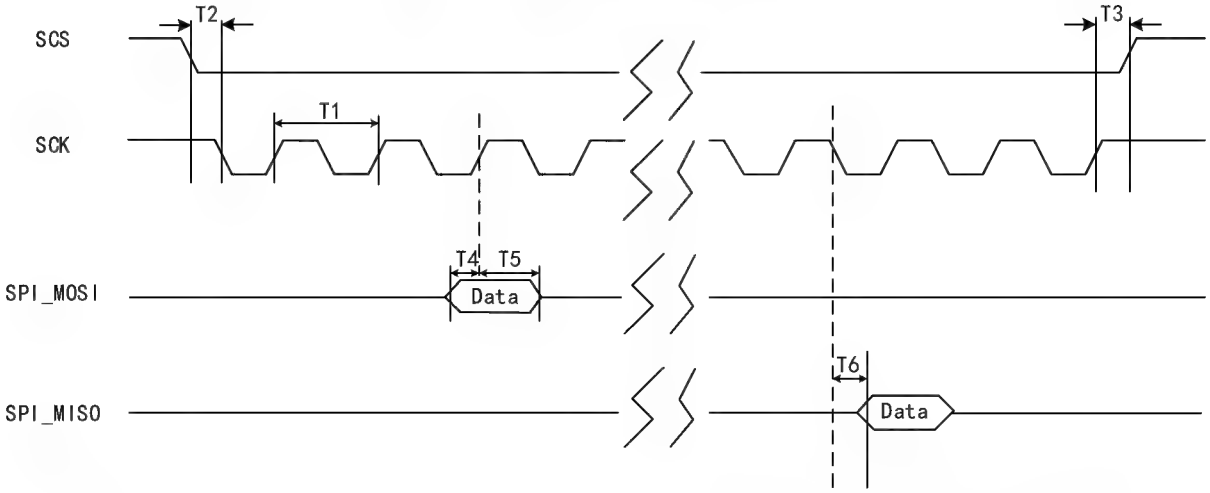


Table 9-5 SPI M3 mode parameter table (AVDD33 = 3.3V, VDDIO = 3.3V, TA = 25°C)

Symbol	Parameter		Min.	Typ.	Max.	Unit
T1	SCK Frequency	VDDIO = 3.3V		50	72	MHz
		VDDIO = 1.8V			64	MHz
		VDDIO = 1.2V			36	MHz
T2	SCS falling edge to SCK falling edge		0			ns
T3	SCK rising edge to SCS rising edge		0			ns
T4	SDI/MOSI build-up time before SCK rising edge		3			ns
T5	SDI/MOSI hold time after SCK rising edge		2			ns
T6	SDO/MISO output delay after SCK falling edge		2		6.5	ns

9.4.2 Oscillator & Crystal Timing

Table 9-6 Oscillator & Crystal timing parameters table

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
TCKF	Crystal Frequency	Recommended within 30ppm	24.999	25	25.001	MHz
TPWH	High clock pulse width		15	20	25	ns
TPWL	Low clock pulse width		15	20	25	ns

Note: The XI and XO pins of the CH390 already have the 2 oscillation capacitors (about 16pF~20pF) required for an external crystal with a load capacitance of 12pF respectively, and only the crystal is required externally. If an external crystal with a load capacitance of 20pF is selected, then XI and XO need to add an additional 15pF oscillation capacitance to ground respectively.

9.4.3 Power On Reset Timing

Figure 9-3 Power-up timing diagram

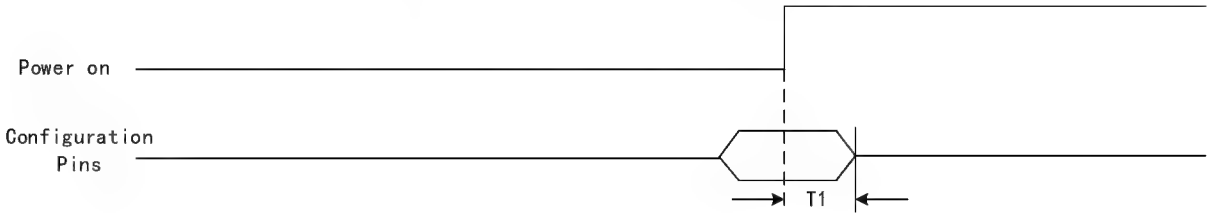


Table 9-7-1 Power-up timing parameters table

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	Configuration pin hold time after power on reset	17	-		ms

Figure 9-4 Reset timing diagram

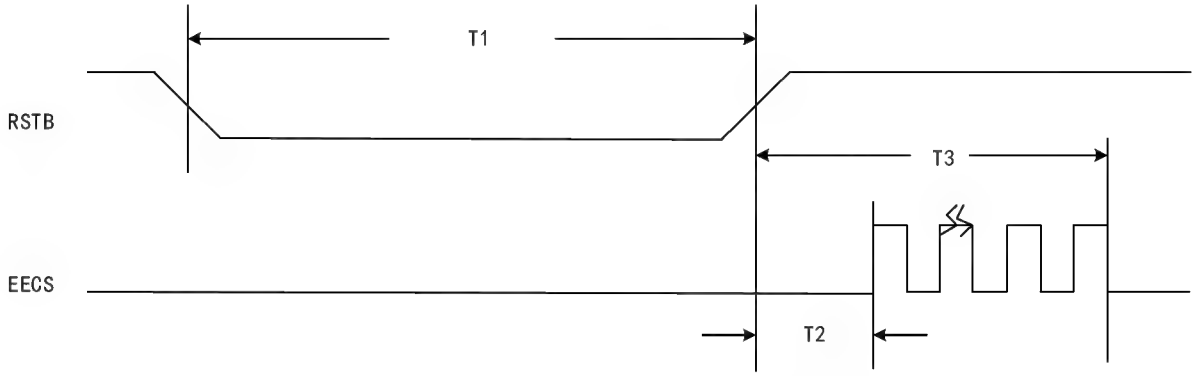


Table 9-7-2 Reset timing parameters table

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	RSTB Low Period	1	-	-	ms
T2POR	Power on reset to EECS high	-	22	25	ms
T2	RSTB high to EECS high	1	-	4	ms
T3	RSTB high to EECS burst end	1	-	4	ms

Note:

(1) Approximately 22ms after power-on reset, CH390 loads configuration values from EEPROM and completes initialization.

(2) Approximately 2ms after RSTB pin reset, CH390 loads configuration values from EEPROM and completes initialization.

(3) It is recommended that the external MCU host or processor access CH390 after 25ms of power-on reset and 4ms of RSTB pin reset.

9.4.4 Parallel Port I/O Read Operation Timing

Figure 9-5 CH390L/F processor I/O read operation timing diagram

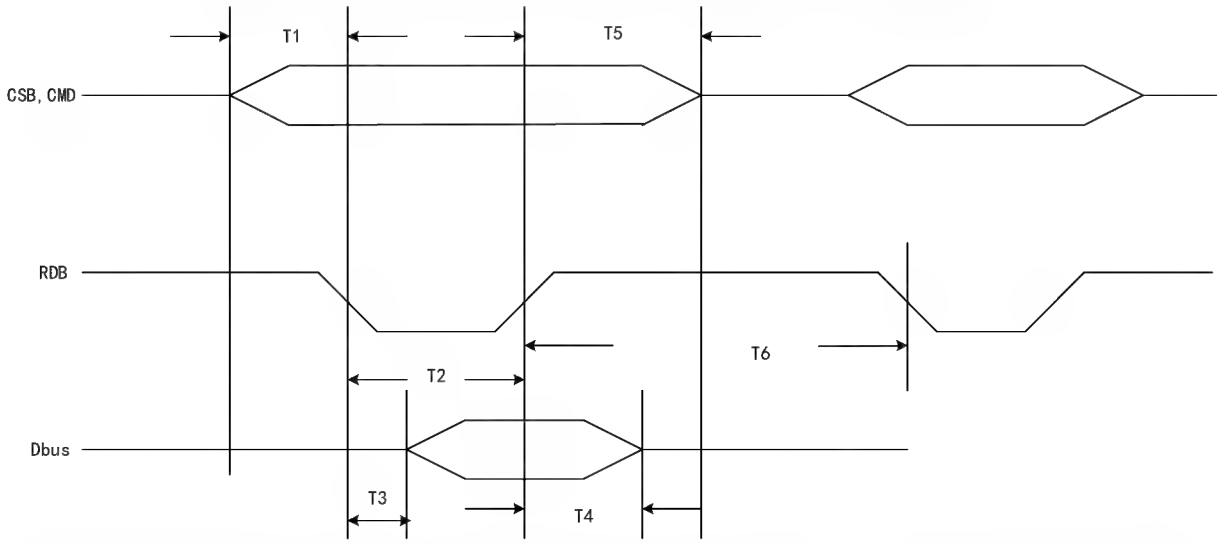


Table 9-8 Parallel port I/O read operation timing parameters table

(AVDD33 = 3.3V, VDDIO = 3.3V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	CSB, CMD valid to RDB valid	0			ns
T2	RDB valid width	20			ns
T3	Data bus (Dbus) output delay time	2		18	ns
T4	RDB Invalid to Data bus (Dbus) Invalid	2			ns
T5	RDB invalid to CSB, CMD invalid	0			ns
T6	RDB is not valid until the next RDB/WRB is valid when the register is read	15			ns
T2+T6	RDB invalid to next IRDB/WRB valid when read memory with F0h or F2h register	30			ns

Note: At VDDIO = 1.8V, the parallel port speed is reduced by 10%; at VDDIO = 1.2V, the parallel port speed is reduced by 50%.

9.4.5 Parallel Port I/O Write Operation Timing

Figure 9-6 CH390L/F processor I/O write operation timing diagram

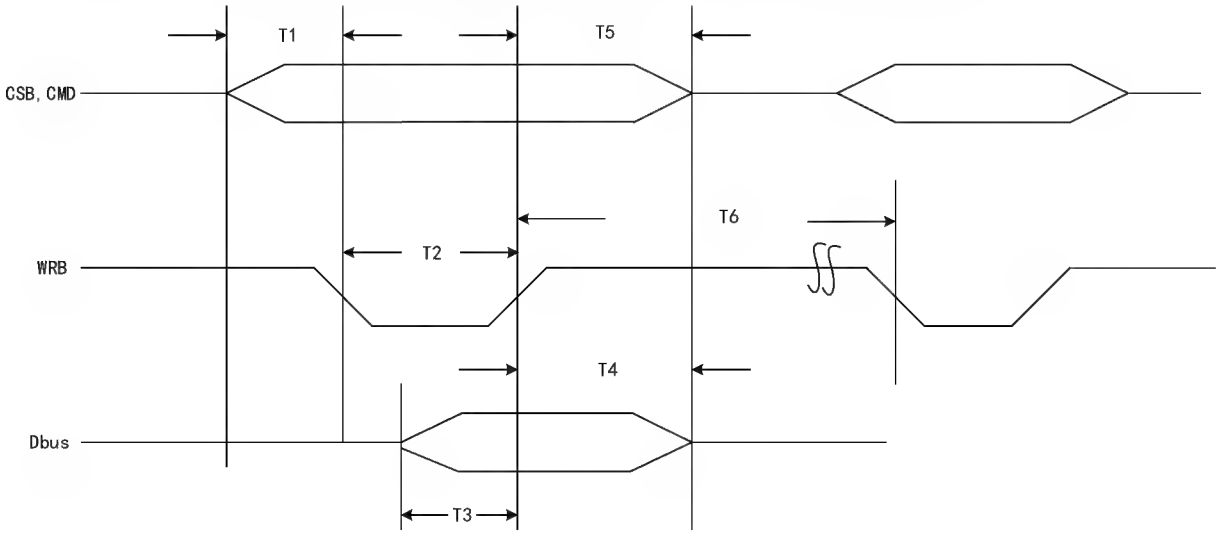


Table 9-9 Parallel port I/O write operation timing parameters table

(AVDD33 = 3.3V, VDDIO = 3.3V, TA = 25°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
T1	CSB, CMD valid to RDB valid	0			ns
T2	RDB valid width	12			ns
T3	Data bus (Dbus) input setup time	8			ns
T4	Data bus (Dbus) input hold time	3			ns
T5	WRB invalid to CSB, CMD invalid	0			ns
T6	WRB invalid to next WRB/RDB when writing to address index or data port	20			ns
T2+T6	WRB valid to next WRB/RDB valid when writing to memory	20			ns

Note: At VDDIO = 1.8V, the parallel port speed is reduced by 10%; at VDDIO = 1.2V, the parallel port speed is reduced by 50%.

9.4.6 Transmission Status LED Switching Time

Table 9-10 Transmission status LED time parameters table

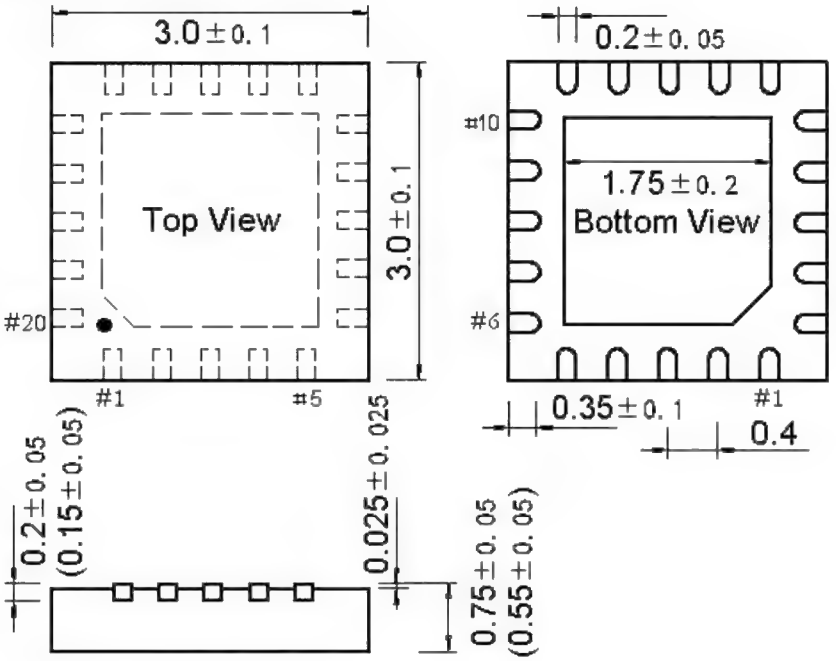
Symbol	Parameter	Min.	Typ.	Max.	Unit
T_{ON}	LED on time when transmitting	-	16	-	ms
T_{OFF}	LED off time when transmitting	120	-	-	ms

10. Package Information

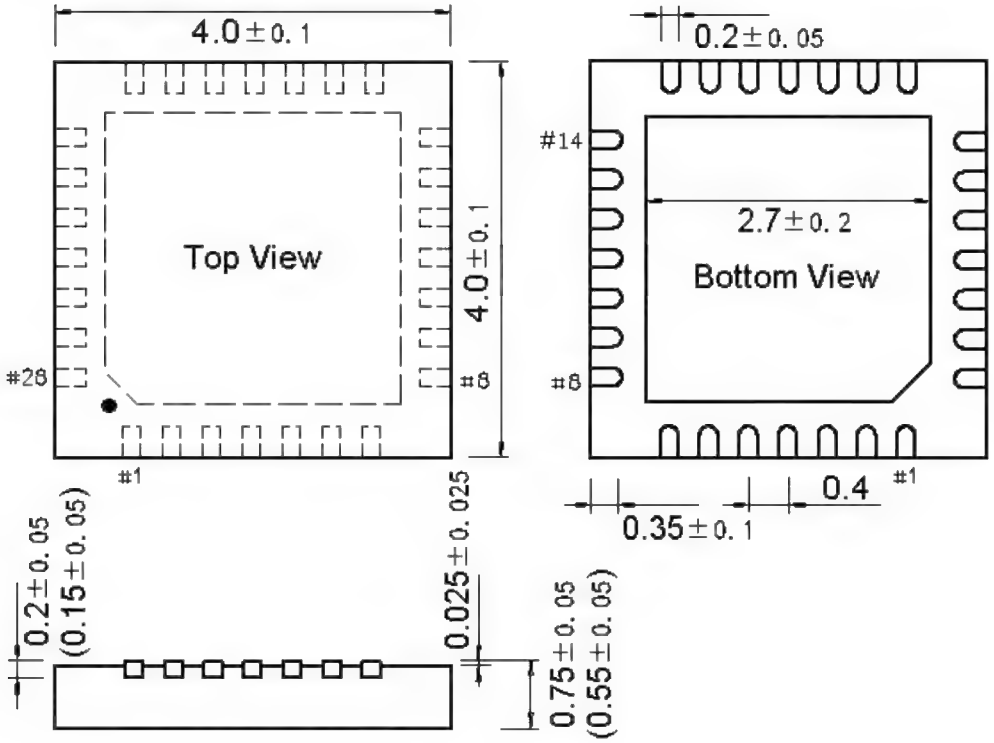
Note: The unit of dimensioning is mm (millimeter).

The pin center spacing is the nominal value without error, and the dimensional error other than that is no more than ±0.2mm.

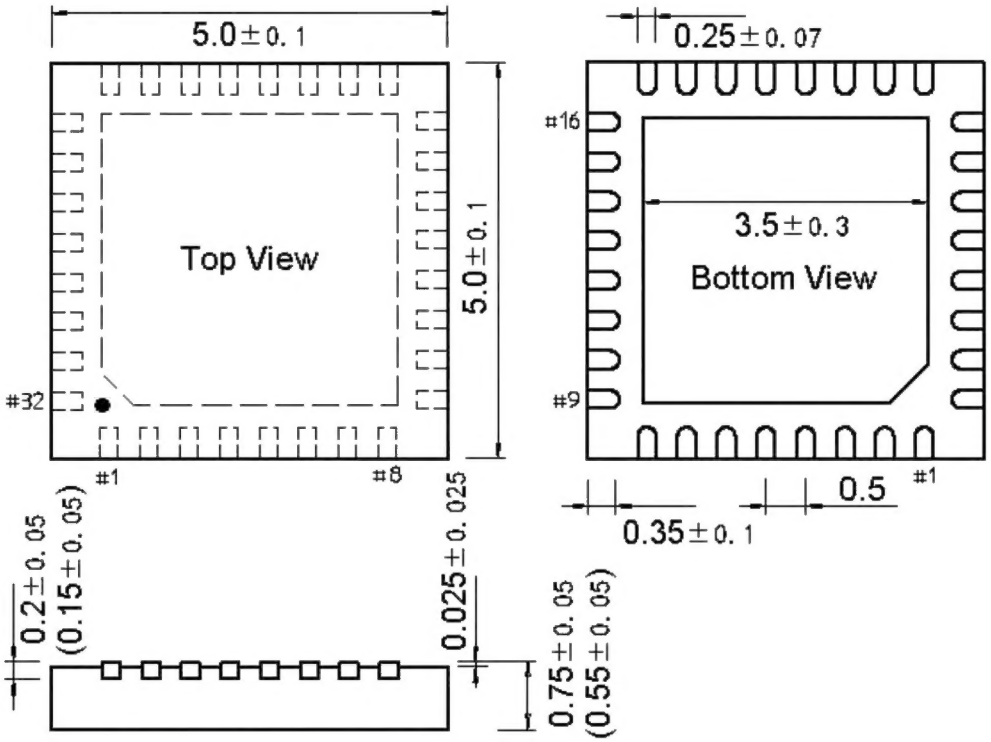
10.1 QFN20 Package



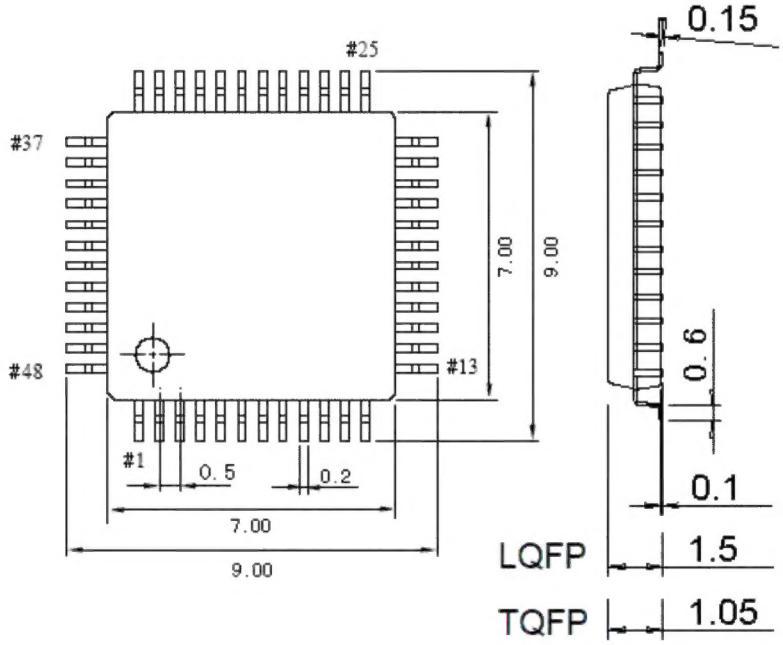
10.2 QFN28 Package



10.3 QFN32×5 Package

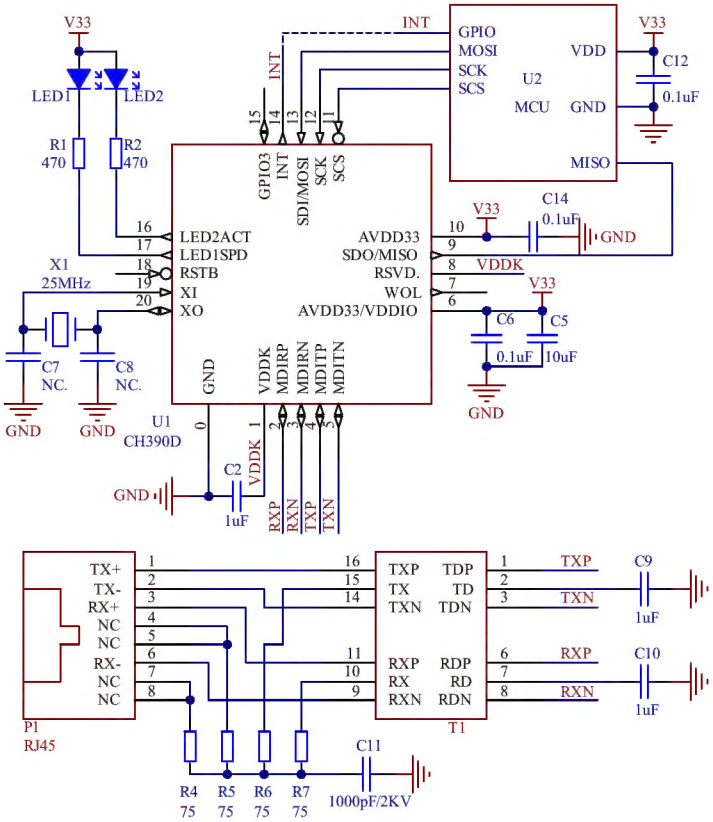


10.4 LQFP48 Package



11. Application

11.1 Single 3.3V SPI Application



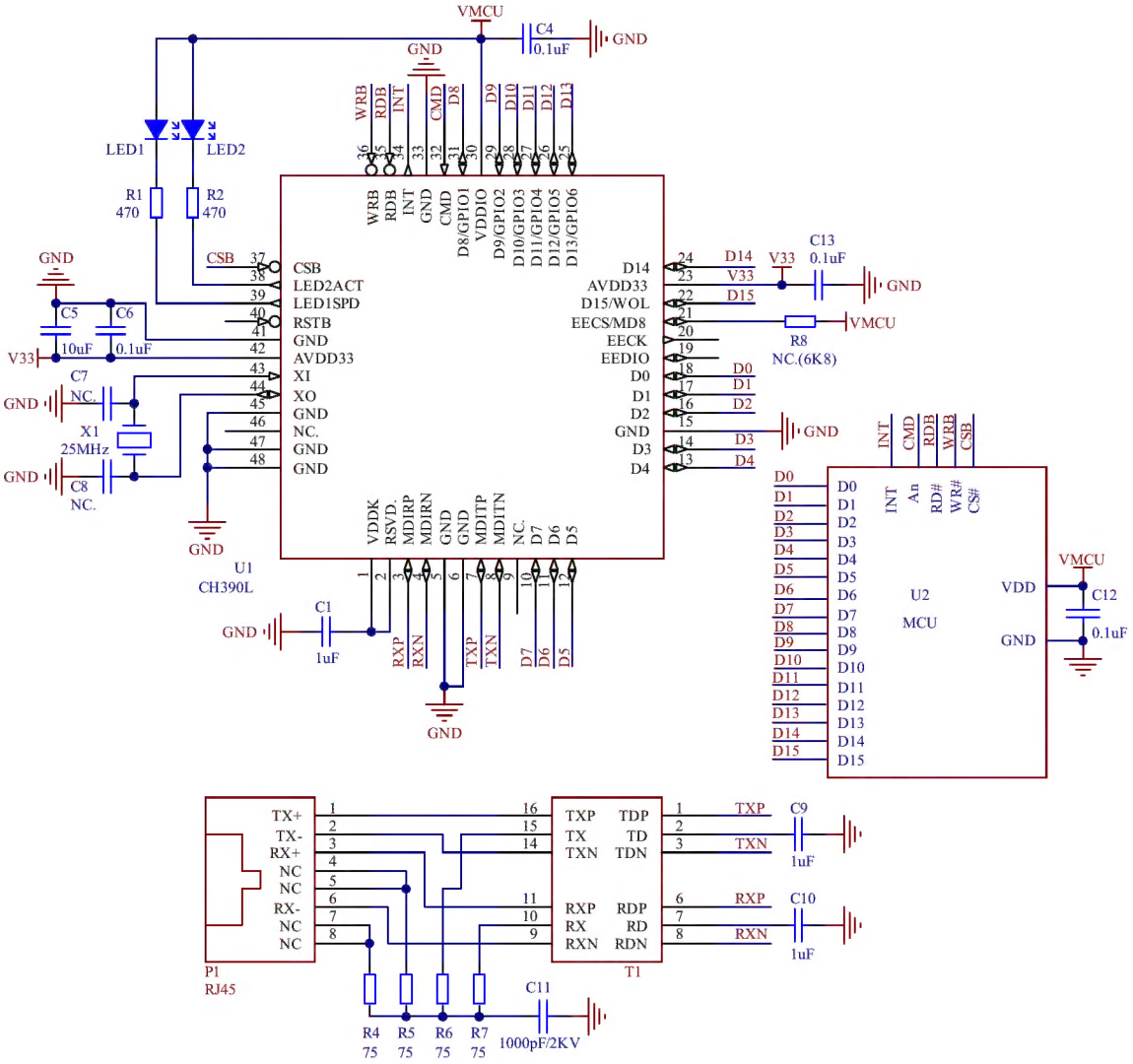
CH390D has built-in part of the oscillation capacitor of crystal X1, and C7 and C8 can be adjusted according to the crystal parameters. For X1 with a load capacitance of 12pF, C7 and C8 are not required; for X1 with a load capacitance of 20pF, C7 and C8 are recommended to be 15pF each.

T1 is an ethernet network transformer. Its center tap is connected to ground through capacitors C9 and C10 respectively. Do not connect to any power supply.

CH390D has a built-in Ethernet 50Ω impedance matching resistor. Do not connect an external 49.9Ω or 50Ω resistor, which is equivalent to voltage drive.

CH390D is smaller in size, and the MCU power supply is also 3.3V. Non-3.3V controllers can use CH390H instead.

11.2 Independent Voltage Parallel Port Application



CH390L has built-in part of the oscillation capacitor of crystal X1, and C7 and C8 can be adjusted according to the crystal parameters. For X1 with a load capacitance of 12pF, C7 and C8 are not required; for X1 with a load capacitance of 20pF, C7 and C8 are recommended to be 15pF each.

T1 is an ethernet network transformer. Its center tap is connected to ground through capacitors C9 and C10 respectively. Do not connect to any power supply.

CH390L has a built-in Ethernet 50Ω impedance matching resistor. Do not connect an external 49.9Ω or 50Ω resistor, which is equivalent to voltage drive.

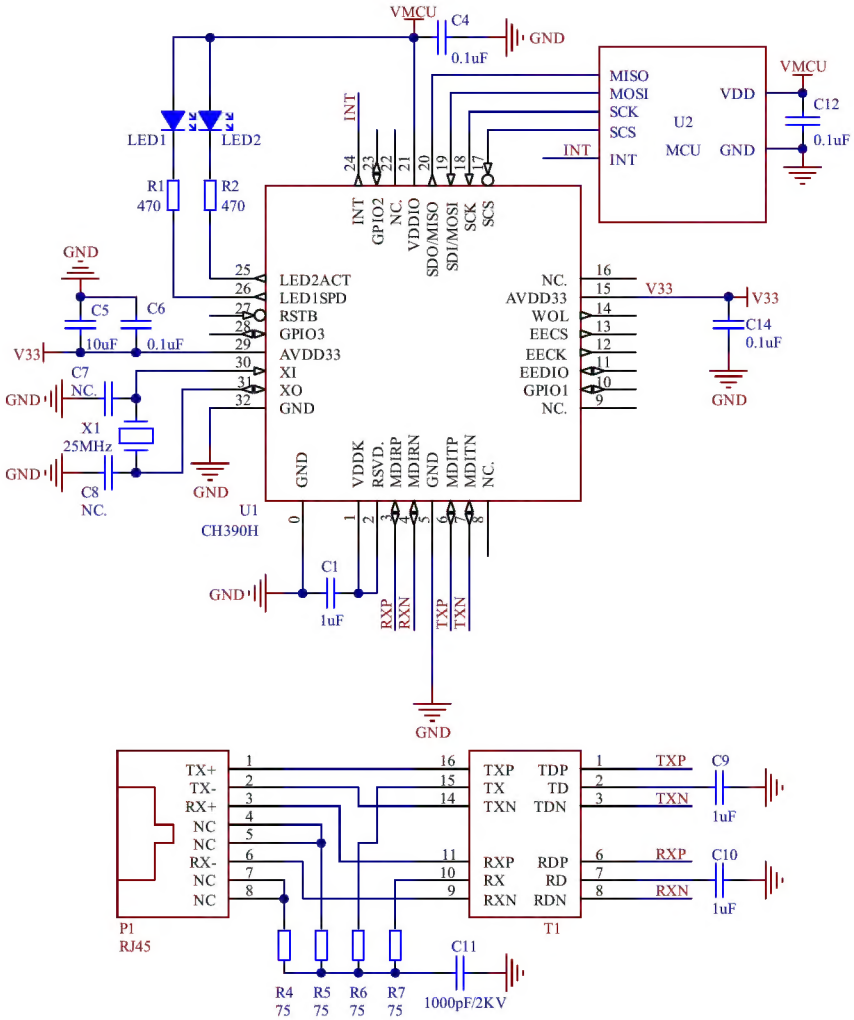
C13 are optional but recommended.

The figure above shows the 16-bit parallel port mode without resistor R8. For 8-bit parallel port mode, resistor R8 is 6K8 or 4K7 pull-up.

The CH390F has been fixed to 8-bit parallel port mode, and its application can be referred to the above circuit diagram.

The CH390 provides a separate I/O interface power supply pin, VDDIO, which supports 3.3V for the CH390L and 3.3V, 2.5V, 1.8V and 1.2V for the CH390F/H.

11.3 Independent Voltage SPI Application



CH390H has built-in part of the oscillation capacitance of crystal X1, and C7 and C8 can be adjusted according to the crystal parameters. For X1 with a load capacitance of 12pF, C7 and C8 are not required; for X1 with a load capacitance of 20pF, C7 and C8 are recommended to be 15pF each.

T1 is an ethernet network transformer. Its center tap is connected to ground through capacitors C9 and C10 respectively. Do not connect to any power supply.

CH390H has a built-in Ethernet 50Ω impedance matching resistor. Do not connect an external 49.9Ω or 50Ω resistor, which is equivalent to voltage drive.

C14 are optional but recommended.